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CORRELATION OF WAFER LEVEL QA TESTS WITH FUNCTIONAL DEVICE YIELD AND ACCELERATED LIFE TEST RESULTS

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13. ABSTRACT (Maximum 200 words)

This report covers work that was to correlate wafer level test structure tests with life tests by utilizing test structures collocated with a RAM-like device. Wafer level tests for oxide breakdown, electromigration, and hot carrier degradation were conducted on a total of six wafer lots from three vendors. Functional testing of the RAM-like device yielded just over six hundred devices to be packaged for the life test. The data from the wafer level and life testing indicate that the oxide breakdown wafer level test is able to be correlated to both functional yield and life test results. This study was not able to conclusively correlate the wafer level electromigration or hot carrier testing to the life test results. Further study with a much larger sample size and a longer life test needs to be performed to further address this issue.

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Correlation of Wafer Level QA Tests with Functional Device Yield and Accelerated Life Test Results

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I: Introduction

Wafer Level Reliability (WLR) testing has become an important tool in the semiconductor industry to monitor wafer production for global reliability hazards. Considerable effort has been devoted to the implementation of WLR tests that produce rapid test results for each targeted mechanism and that have been shown to correlate well with long term mechanism specific tests. Some of these wafer level tests have been accepted as Joint Electron Devices Engineering Council (JEDEC) standard test methods, while others are in the process of being considered. Having standard test methods goes a long way toward transportability of test results between fabricators, but the designers are still faced with the concern that the design sensitive aspects of wear-out have not been adequately proven to be addressed by the WLR tests.

When Application Specific Integrated Circuit (ASIC) designs are created with libraries of standard logic blocks it is possible to address the design sensitivity issues of wear-out. By using the concepts outlined in the Qualified Manufacturers List (QML) procedures (MIL 38535), it is possible to utilize WLR test structures to assess the presence of global early wear-out processes that will influence the probable reliability of parts in a wafer lot containing ASIC devices implemented with a qualified standard cell library. A necessary link in building confidence in the assertion that WLR testing can be used to assess the probable reliability of the product on the wafer lot is that a correlation between WLR test results and long term life tests, conducted on an appropriate ASIC device, must be performed.

Controversy exists over whether test structures have any real basis for use in predicting the expected lifetime of integrated circuits based upon differences in area, processing, and stress seen by the test structure versus an ASIC device. A step in the direction of addressing this controversy may be made by taking advantage of some earlier work in wafer level reliability test structure development, in which six wafer lots were fabricated with extensive wafer level reliability test structures along side a simple functional device designed using a DoD CMOS cell library. It is an opportunity to gain insight into the relationship between WLR test results and a specific ASIC design yield and lifetime in a burn-in like accelerated test. By testing the wafer level reliability test structures on each wafer using current JEDEC test methods (proposed and approved), we are able to see if there is a connection between wafer level test results, yield and reliability (under burn-in like conditions). These results are for three different fabricators and for

wafer lots fabricated at up to three different times from the same fabricator which allows us to check for lot to lot consistency. From this work, we may show the degree to which there is a connection between wafer level test results and functional ASIC yield and reliability.

Wafer Lots Used for this Effort
(Lot Fabrication Date)

Vendor A	Lot A (1/88)	Lot B (7/88)	Lot C (9/88)
Vendor B	Lot E (8/88)	Lot F (11/88)	----
Vendor C	Lot D (5/88)	----	----

II: Test Structure Descriptions: Overview

This section will provide details on the test structures used for the wafer level reliability (WLR) testing and on the self-exercising circuit that was used as the functional device in the yield and life tests. To whatever degree possible the WLR test structures were designed to standards that are being considered by JEDEC. Since these WLR structures were designed and fabricated before the JEDEC WLR Task Group was formed there are some deviations from the proposed standard test structures. In this particular case, the fact that the test structures are slightly different from the JEDEC WLR structures is of no consequence because we are making a relative comparison between three different fabricators and up to three different fabrication lots from a single fabricator.

Our goal is to show correlation between functional ASIC devices and WLR test structures and not the relative sensitivity of the WLR structures used in this effort and in the JEDEC proposed standards. However, since there are only small differences between currently proposed JEDEC WLR structures and the WLR structures used for this work, we should expect that similar test results would be obtained with the JEDEC structures when the standards are agreed upon. The following description of the WLR structures used in this task will make this point fairly clear.

There are two general categories of devices fabricated on the wafers used in this task: 1) WLR test structures. 2) A self-exercising ASIC device with a high degree of testability.

The WLR test structure chip, shown in Figure 1, has a number of different WLR test structures that were used in test structure evaluations. Within that chip are arrays of transistors for hot carrier testing, Time Dependent Dielectric Breakdown (TDDB) test capacitors configured in two different design styles, and electromigration test structures ranging from standard ASTM (American Standard Testing Methods) standard test structures (formerly National Institute for Standards and Technology, NIST, test method) for oven based testing at moderate acceleration factors to Standard Wafer-level Electromigration Accelerated Test (SWEAT) structures for rapid wafer level electromigration testing.

The second category is the ASIC device that was used for the life test after the WLR structures were tested and the data analyzed. This ASIC device was designed using the CMOSN library cells (a CMOS cell library using a scaleable set of design rules supplied by the DoD) that are characterized for the feature sizes used in the fabricated lots used for this task. The Self-Exercising Circuit (SEC), shown in Figure 2, is organized so that it may be exercised in either a self-oscillating or a clock driven mode. In addition, the individual cells within the SEC array can be accessed in a RAM-like manner, to allow identification of an individual failed cell. The self-oscillating frequency is sensitive to changes in transistor g_m (as well as V_{DD}) and is used as one means for assessment of the existence of hot carrier damage.

III: Test Structure Descriptions: WLR Structures and Test Procedures

A: Test Structures

Electromigration:

Test Structure: Within the WLR test chip shown in Figure 1, there are NIST (ASTM standard) electromigration structures and an early version of the SWEAT test structure. The SWEAT structure, found in the second to last row, is of primary interest in this study because it is very similar to a JEDEC proposed standard. The only significant deviation of this structure from the JEDEC structure is that the voltage taps are located in the probe pads some distance from the repetitive structure. This difference has little effect upon the relative comparisons that were made in this correlation study. The test procedure used is the same method as is in the JEDEC proposed method.

Test Procedure: A closed loop test procedure is the preferred wafer level electromigration test procedure. This method involves ramping the stress current up to a level that causes an acceleration factor, due to both current density and temperature (temperature rise by Joule heating), to reach a value that will lead to a median time to fail on the order of 30 seconds, and holding this stress factor constant until the metal test structure fails open. This method involves calibrating the material from each individual fabricator, and as a result, it is not possible to compare one fabricator with another. However, it is possible to compare variations in median time (and sigma) to fail from wafer to wafer and from lot to lot.

A measure of "absolute" metal electromigration quality is only obtainable from the straight line tests that use the standard ASTM test structure and test method, which requires several hundred hours of at-stress testing to compile a metal reliability data base. Generally this method is the basis for comparing one fabricator with another. In this task we are primarily concerned with metal quality variations between wafer lots and between wafers within a lot, so the longer test is not required.

The SWEAT test results were used primarily as an indication of general metal quality. In cases where there were wide variations of sigma or median time to fail, we looked for life test indications of electromigration damage.

Hot Carrier Damage:

Test Structure: Two rows of isolated hot carrier test transistors (one row of N-channel and one row of P-channel) are found on the test chip in Figure 1.

Test Procedure: Since there is no currently accepted JEDEC standard for hot carrier damage testing, we selected a common method that uses DC measurements of drain current at the maximum substrate current. This method involves measuring the drain and substrate current as the gate bias voltage is varied, until the peak substrate current is reached. The ratio of the resulting peak substrate current and the measured drain current, I_{sub} / I_{DD}, is used as a relative quality factor for hot carrier damage susceptibility. This method is only useful as a relative rate of hot carrier generation monitor (using re-combination current) for wafer production and is not a direct measurement of the actual damage that is taking place. It provides a simple wafer level method of testing changes in transistor manufacturing that may result in an excessive damage rate, relative to some reference rate, as determined from transistors designated as a reference for the hot carrier damage rate.

A direct measurement of the accumulation of hot carrier damage is possible using a method from the literature which involves using charge pumping measurements to detect changes in the interface states. As hot carrier injection produce an increased number of interface states, this method will directly measure changes in the number of interface states. It is a very sensitive detector of the accumulation of hot carrier damage and may detect changes in the damage rate before it is observable with I/V measurements. Measurements were made using the charge pumping technique to determine if a sufficient damage rate to be observable in circuit performance existed.

Time Dependent Dielectric Breakdown:

Test Structure: The wafers used in this task contain two different arrays of TDDB test capacitors. One array consists of 32 long rectangular capacitors that were used in some early studies in test methods for TDDB. These capacitors are significantly different in layout than the JEDEC recommended layout for test capacitors. The second capacitor type is generally in agreement with the JEDEC recommended layout and were used in this study even though the available sample size is smaller. These test capacitors are located on the left side of the reliability test chip. However, because of the relatively small number of capacitors per test chip, there will not be enough structures per wafer to distinguish wafer to wafer variations within a wafer lot. By testing within the JEDEC standard guidelines, we may extract useful gate oxide defect density information that will be more directly correlatable with the functional devices.

Test Procedure: There are two JEDEC standard TDDB test methods available: Current-Ramp and Voltage-Ramp. The choice of one versus the other is determined by the degree of sensitivity that is required for the oxide study.

Current-Ramp tests are most useful for distinguishing small differences between nearly intrinsic quality (i.e., nearly defect free) gate oxides. The test begins by forcing a specified level of constant current (defined in the JEDEC standard) through the oxide and then increase the current in a linear manner until the oxide fails. The time required for the Current Ramp test is relatively short because the test begins at a moderately high oxide current density, which is significantly greater than normal operating conditions.

Voltage Ramp testing uses a linear ramp voltage force beginning at a voltage level equal to the nominal operating voltage of the CMOS devices. Voltage is increased at a prescribed ramp rate (rate defined in the JEDEC standard) while monitoring the capacitor current. When the current increase through the capacitor is greater than normal Fowler-Nordheim level the voltage level is logged to indicate failure. The Voltage Ramp test is most useful when the oxide quality is unknown. Test time is longer than with the Current Ramp method because stressing begins at nominal operating field and is ramped to failure.

Since we expected wide differences in gate oxide quality, the JEDEC Voltage-Ramp was chosen for this task. This method has broader dynamic range for being able to deal with both high and low defect density oxides. The only significant disadvantage of the Voltage Ramp method is that it requires greater time to run the tests. This limitation is not serious for this task. The primary goal was to be able to rank the various oxide defect qualities between the different wafer lots.

Self Exercising Circuit (SEC):

Test Structure: The Self Exercising Circuit was designed to facilitate the process of evaluating the nature of any life test failures that occur. The general architecture of the SEC is shown in Figure 2. This chip was designed using the DoD CMOSN scaleable standard cell library. This allowed us to use a well characterized cell based design which provided a sound basis for evaluating both yield and reliability from many different fabricators at many different feature sizes. This was important because the wafer lots used in this task were fabricated at three different contractors and two feature sizes (2.0 μm and 1.6 μm) in order to provide diversity in the WLR test structure evaluations.

An additional feature of this version of the SEC is that there were two versions of the SEC fabricated on the 2.0μm CMOS runs: a) One version that was designed specifically with a 2.0μm version of the CMOSN cell library, and b) Another version that was a global scale up from the version designed for the 1.6μm CMOS technology. The scaled up version results in an identical array to the 2.0μm version, but the pads are slightly larger scale which makes the chip area

around the pad frame slightly larger. We did not expect to see any significant yield difference between these two versions of the SEC.

The SEC is a reconfigurable array that may be operated as a very large ring oscillator, a very long delay inverter delay line, or as an addressable structure which allows checking for functionality in each array cell. This allows the array to be either self-stimulating in the ring oscillator mode or be driven by an external signal that appears on the DIN port. The XMUX and the YMUX allow the majority of the chip circuitry to be accessed such that it is possible to identify a faulty cell.

Test Procedure: Referring to Figure 2 the MUX BIT is the basic array cell (a two input multiplex cell) and is arranged as either column connected or row connected elements. In the column connected mode it can operate as an array of parallel inverter delay lines with access to each column through the YMUX structure at the bottom of the columns. The first row of MUX BIT cells serves a special function that allows the output of the last element in the column (column n) to be connected to the next column (column n+1), such that all of the cells in the array are connected in series. The number of MUX BIT cells in each column is an even number so that the output of the column is a delayed replica of the column input signal.

An input control signal (HB_V) causes the serial connection of the array cells when its logical value is zero. Having a net non-inversion in each column results in there being a non-inverting output from the last column in the array delayed by the total number of cell delays in the array. By adding one more inversion, external to the array, we can cause the network to self-oscillate. The self-oscillation frequency is determined by the average transistor conduction characteristics of all of the transistors in the MUX BIT array. This mode can be used to determine if there has been a significant change in g_m, caused by hot carrier damage, to the N-channel transistors in the array. Self-oscillation can also be used to exercise the cells in the chip at relatively low frequency (around 300KHz to 400KHz).

When HB_V is a logical one an input signal may be used to drive the array at any clock frequency desired. In this task, we used a 5.0MHz clock signal to drive the array. This frequency was chosen because it causes the array to demand a significant power supply current (about 50 mA 5.0 at Volts V_{DD} and about 70 mA at 7.0 Volts V_{DD}) that will serve nicely to exercise the chip for electromigration susceptibility.

When self-oscillation and external stimulus is disabled, the array can be configured for testing by either placing the first row of MUX BIT cells in vertical propagate mode and testing for column propagation through the YMUX, or by placing the array of MUX BIT cells in horizontal propagation mode and testing for horizontal propagation through the XMUX. Any cell in the array that fails to propagate may be located by the intersection of the failed row and column in the above test. In its present form there is no way to separately test the XMUX and YMUX circuitry. However, since this XMUX and YMUX circuitry is a very small percentage of the total array area, it is far more likely that defects will be found in the MUX BIT array.

B: Test Flow:

Wafer level reliability testing was performed using a Keithley Model 450 parametric test system. Wafers were probed and the data statistically analyzed to extract information that could be used to attempt to predict the results of the functional testing.

The functional testing was performed in two phases: 1) at wafer probe to identify all functional SEC chips and to map wafer positions that will be packaged for the life tests, and 2) Post packaging functional tests on the SEC to detect any additional failures that occurred in packaging, and to provide an accurate accounting of all initially good SEC chips.

A sequence number was written on the packages for identification in subsequent testing. Each SEC used in the life tests was thoroughly tested for functionality before insertion into the life testing boards.

IV: Wafer Level Reliability Test Results

Wafer level reliability testing produced some rather interesting results that turned out to be both beneficial and detrimental to the goals of this task. We found that the metal electromigration quality and gate oxide quality was widely variable between the three wafer fabricators. This had the benefit of providing an opportunity to see the degree yield and reliability is predictable from WLR test results. However, it had the disadvantage of leading to poor SEC yield on lots that had poor gate oxide quality. This meant that the number of available SEC chips was seriously limited, which impacts the ability to arrive at good statistical results.

Hot Carrier Damage:

Hot carrier testing yielded very little useful differences between wafer lots or between fabricators. Referring to the plot in Figures 3a, 3b, 3c, and 3d, we can see a typical set of hot carrier data from a wafer lot used in this task. The data is plotted to maximize visibility of the differences between the measured transistors. Only tests performed at a drain voltage of 7.0 Volts are shown (Note: Transistors on Lot E and Lot F had oxide breakdown at 7.0 Volts, so no high stress factor hot carrier data is available from these lots). Variations from wafer to wafer and lot to lot show that hot carrier damage is not likely to be a reliability limiter in any SEC devices from these lots. Even though there is no absolute current ratio that clearly indicates a lot with poor hot carrier damage resistance, it is clear that there is no way that the life tests that we ran in this task will show any statistically significant differences between these lots.

The fact that the results obtained here are statistically inconclusive does not allow us to conclude that hot carrier damage is not a significant reliability limiting consideration in general. The results obtained here only indicate that for the wafer lots used in this study, it is not possible to measure differences between the lots. It is also not possible to assign an absolute hot carrier damage reliability figure to this set of wafer lots because there is no model that will accurately extrapolate these results to at-use conditions.

Electromigration:

The SWEAT test procedure chosen was the proposed JEDEC standard method. The test results were compared on a wafer to wafer basis to observe any quality variations that may be present. A major goal of this work was to determine to what degree the wafer level electromigration tests (SWEAT in particular) can be used to distinguish between good and poor metal systems from a given wafer fabricator. SWEAT testing will not be able to distinguish quality variations between fabricators, because there is a fabricator specific calibration performed to standardize the SWEAT median fail times to 30 seconds. Some earlier package level tests were used to provide a more fundamental metal characterization comparison between fabricators.

Package level test results show some fundamental differences between fabricators. The Vendor A metal systems show superior electromigration lifetime at package level testing. Vendor C test

results were not available because there were not sufficient test chips from the single wafer lot to perform a statistically significant test. Vendor B test results were not obtained because there were a large number of metal failures in the chip heater. The heater failures occurred at temperatures above 250°C, which made it impossible to run a complete series of tests required for evaluating parameters needed for comparison between fabricators. A comparison of electromigration test results from Vendor A and Vendor B at a single temperature (three temperatures at a single current density are a minimum for evaluation of activation energy) shows very short t_{50} for Vendor B at significantly lower current density.

Vendor A at J=3.0 X10^6 A/cm^2, T=250°C resulted in
t_{50}=51.4 hours, σ=0.50.

Vendor B at J=7.5 X10^5 A/cm^2, T=250°C resulted in
t_{50}=11.2 hours, σ=1.3.

It is not clear why the Vendor B lots have such poor electromigration performance, but it is an opportunity to see if these results are reflected in life test results even though it is not possible to compare metal reliability performance directly in package level electromigration tests.

SWEAT test results indicated no significant lot to lot or wafer to wafer variations for Vendor A. Median time to fail variations and sigma variations were not sufficiently large to be statistically significant. SWEAT test results for Vendor C can only show within lot wafer to wafer variations in metalization quality. Wafer to wafer sigma variations for SWEAT tests on Vendor C were slightly higher than for Vendor A wafer-to-wafer variations within each lot of Vendor A. Based upon these SWEAT results for Vendor A and Vendor C plus the package level test results for Vendor A, we would expect that there would be very few, if any, electromigration failures on Vendor C SEC devices, and we would expect none from Vendor A SEC devices.

The most interesting electromigration test results were from Vendor B. As indicated above we were unable to conduct complete package level tests because metal connections to the on-chip heater show rapid electromigration failures. In addition the SWEAT test results were very erratic. Referring to Figures 4a - 4f it can be seen that there are wild variations in the t_{50} results from SWEAT testing. Sigmas were reasonably small, but the median time to fail data indicates a substantial wafer to wafer variation in metal quality. The data given for this run (Lot F) is typical of the other wafer lots from Vendor B.

We concluded that, based upon these electromigration test results that the Vendor B wafer lots would have significant signs of electromigration damage, possibly including some open metal failures, in the SEC devices operated in the test oven at 175°C.

Time Dependent Dielectric Breakdown:

The JEDEC standard Voltage Ramp test was chosen for this study to make it possible to analyze widely varying test results. A disadvantage of the Current Ramp test is that it presumes good oxide and is used to resolve small variations from lot to lot while investing a minimum of test time. This study had to assume that there would be wide variations in oxide quality and that the test results could be used for comparison purposes between fabricators.

The test structure that was chosen had two structures per site on each wafer. Since we needed to resolve the defect tail of the distribution over a wide range of oxide qualities the number of test capacitors must be at least 100. This constraint means that it will not be possible to look for wafer to wafer variations. However, for purposes of oxide defect related yield, it is sufficient to only resolve differences between lots.

A great deal may be learned about the oxide quality from the Voltage Ramp test results. This test resolves types of failures that enable an assessment of initial defect caused failures and an assessment of the defect distribution to be made. TDDB testing involves an initial test at 5.0 Volts, a Voltage Ramp test, and a final post-stress test. The post-Voltage Ramp failure categories are shown in Table 1.

Table 1: JEDEC V_Ramp Failure Categories

Failure Category	Initial Test	V_Ramp Test	Post Stress
1) Catastrophic	Pass	Fail	Fail
2) Masked Catastrophic	Pass	Pass	Fail
3) Non-Catastrophic	Pass	Fail	Pass
4) Others	Pass	Pass	Pass
5) Initial	Fail	X	X

Initial Test Failures provide information about the effect of the defect tail upon the yield of oxide areas of 72,000 μm^2 or larger. If this initial test yield is poor, then it is reasonable to assume that functional devices will not yield well due to oxide defects. A failure in the others category indicates a miss-probe and is censored from the statistics. A masked catastrophic failure indicates that there may be an instrument timing problem, which caused the equipment to miss a failure during the Voltage Ramp test. The masked catastrophic result is also censored from the statistics in this study. Finally, a non-catastrophic failure indicates that there was an initial short circuit fail that later opened. We also censored these results from our TDDB data plots, which, as a result of all of the above, contain only catastrophic failure category data.

Initial Fail (Category 5) TDDB test results for the lots tested are found in Table 2.

Table 2: Initial Fail Data for Area Capacitors

	N-Chan	P-Chan	ΣN+P/# wafers	Notes / # wafers
Lot A Vendor A	3 (239)	33 (269)	8.75 / wafer (1.0 / wafer)	4 wafers in the lot.
Lot B Vendor A	18 (434)	5 (105)	3.3 / wafer	7 wafers in the lot.
Lot C Vendor A	3 (570)	2 (606)	0.56 / wafer	9 wafers in the lot.
Lot D Vendor C	58 (705)	44 (700)	11.3 / wafer	9 wafers in the lot.
Lot E Vendor B	77 (251)	41 (208)	23.6 / wafer	5 wafers in the lot.
Lot F Vendor B	150 (506)	26 (412)	14.7 / wafer	12 wafers in the lot.

The Initial Fail Data for Area Capacitors in Table 2 is an indicator of the density of fatal defects in gate oxide. Since the capacitor area is only 72,000 μm^2, there should be a very small percentage of initial failures if the gate oxide defect density is very small. Because of the fact that these wafers were used as part of another funded task the number of available untested capacitor samples is variable. The columns headed by "N-Chan" and "P-Chan" show the number of failed capacitors and the number of capacitors in each sample category is shown in parenthesis. A rough indicator of gate oxide defect density is given in the column headed by "ΣN+P/# wafers" and is simply the number of defective capacitors (the sum of N-Chan and P-Chan) divided by the number of wafers in the lot. The last column indicates the number of wafers in each lot.

Distribution of initial failures was generally uniformly distributed over all of the wafers in the lot. The one exception was wafer number 7 in Lot A, which has an unusually high number initial failures in the P-Channel capacitor. There is no obvious reason for this result. If we consider the wafer 7 P-Channel capacitor observations as outliers, then the average number of defective capacitors per wafer (shown in parenthesis in the column headed by "ΣN+P/# wafers" in the Lot A row) is more typical of Vendor A.

With the exception of the anomalous behavior of wafer 7 in Lot A, the Vendor A lots show far fewer initial defects per wafer than either Vendor C or Vendor B. From these results we estimated that the SEC chip yield from the Vendor A lots would be far greater than either Vendor C or Vendor B.

The Voltage Ramp test results are very striking. Figures 5a - 5f contain the Voltage Ramp test results for the entire lot. Each Figure contains a group of six plots on each graph representing all combinations of N/P channel area, poly edge and field edge capacitors. Capacitor sample sizes

are generally greater than 100 for all types and lots as shown in the legend at the bottom of the figures. All failures are in the catastrophic category. Other than the Initial Failure Category indicated in Table 2, there were no other categories of failure observed in the Voltage Ramp test performed in this task.

All of the Vendor A lots (Lot A, Lot B, Lot C in Figures 5a - 5c respectively) show no recognizable defect tail in the Voltage Ramp breakdown and have a median (intrinsic)failure field on the order of 8 to 10 MV/cm. This is further evidence that the number of oxide defects is rather small. The SEC devices from these lots will likely have high yield and are not likely to show significant life test failures attributed to TDDB. There is not sufficient area in these test capacitors to measure the defect tail on these wafer lots.

The Vendor C wafer lot (Lot D Figure 5d) shows a median intrinsic breakdown field on the order of 8 to 10 MV/cm, similar to what was seen in the Vendor A lots. However, there is definite evidence of a defect tail extending down to a little over 3 MV/cm. The intrinsic population is not as tightly grouped as the Vendor A lots. This would indicate that there will be a decreased SEC yield relative to the Vendor A lots. It also indicates that there may be a significant number of life test failures, because of the higher average defect density indicated by the presence of the defect tail.

Vendor B wafer lots (Lot E and Lot F, in Figures 5e and 5f)are dramatically different from the above wafer lots. There is essentially no tightly distributed tightly grouped intrinsic component to the failure distribution. The entire failure distribution is widely spread from the operating field up to about 10MV/cm, suggesting that the failures are strongly dominated by defect related failures. These results indicate the likelihood that there will be a very high SEC yield loss due to oxide defects.

V: SEC Wafer Probe and Package Yield:

After all of the WLR testing was completed the SEC's were probed to determine their yield at the wafer level. All non-yielding SEC devices were inked to identify them to the packager, so they would not be packaged. Each yielded SEC was packaged in a 28-pin hermetically sealed side based ceramic DIP to MIL-883 specifications. Packaged SEC devices were tested again to eliminate any devices that yielded at wafer level, but failed after packaging. Life tests were run only on SEC devices that passed both wafer level and package level functional tests.

The SEC test procedure consisted of first placing the chip into self-oscillation mode and measuring the frequency, power supply voltage and current. If the chip failed to oscillate, it was assumed failed and was marked non-yielded. After a chip passed the self-oscillation test, it was placed into the mode that permits full scan of the entire array of cells and tested for stuck-at faults. If any row or column failed to pass data, the chip was marked as a non-yielded device. SEC chips that have passed both tests were then packaged.

A. Wafer Probe Test Results:

SEC wafer probe test results provide the first look at the possible correlation between yield and WLR test data. Note that Lots D, E, and F contain two versions of the SEC: one version which was scaled up from the 1.6μm to 2.0μm (indicated as JA and HA in the table entries) and the other version which was directly designed as a 2.0μm chip (indicated as JB and HB). The SEC yield is summarized in Table 3.

Table 3: SEC Wafer Probe Yield

Waf. No.	Lot A	Lot B	Lot C	Lot D (JA)	Lot D (JB)	Lot E (HA)	Lot E (HB)	Lot F (HA)	Lot F (HB)
1	19/30	20/30	22/30	3/21	9/32	4/14	0/14	8/17	0/17
2	17/30	19/30	19/30	3/21	7/32	7/14	0/14	6/17	0/17
3	18/30	20/30	19/30	4/21	6/32	5/14	0/14	7/17	0/17
4	18/30	22/30	15/30	2/21	9/32	10/14	0/14	5/17	0/17
5	14/30	18/30	15/30	3/21	8/32	4/14	0/14	7/17	0/17
6	19/30	20/30	18/30	1/21	9/32	5/14	0/14	8/17	0/17
7	-----	17/30	21/30	3/21	13/32	5/14	0/14	7/17	0/17
8	-----	22/30	17/30	3/21	6/32	5/14	0/14	1/17	0/17
9	-----	19/30	14/30	3/21	10/32	1/14	0/14	2/17	0/17
10	-----	16/30	14/30	-----	-----	6/14	0/14	5/17	0/17
11	-----	-----	-----	-----	-----	-----	-----	6/17	0/17
12	-----	-----	-----	-----	-----	-----	-----	6/17	0/17
Lot Yld.	105/180 (58.3%)	193/300 (64.3%)	164/300 (54.7%)	25/189 (13.2%)	77/288 (26.7%)	52/140 (37.1%)	0/140 (0%)	68/204 (33.3%)	0/204 (0%)

The most striking observation it that the SEC yield from the Vendor A lots (Lot A, Lot B, Lot C) were greater than 50%, while the other lots generally yielded less than 37%. The TDDB test results at wafer level predicted that the Vendor A lots would yield well compared to the other lots, because the gate oxide defect density was significantly lower. Since there were very few cases where chips failed because of obvious intra-layer shorts, it may be reasonable to assume that most of the yield failures were due to defects in the gate oxide.

The next observation is that the 2.0μm version (HB) of the SEC did not yield at all in Lots E and F, yet the scaled up version (HA) yielded at least 33%. There is no obvious explanation for this strange result. There is nothing in the geometry of either the scaled or unscaled version (No Design Rule Check, DRC, errors in either design) of the SEC to suggest this odd split in yield. A significant clue to the nature of the failures on the non-yielded 2.0μm version (HB) is that all of the failed chips show very large power supply current, suggesting either metal to metal shorts or latch-up. No effort was expended to determine the cause of the large current failures, because it

is likely that some sort of geometry error unrelated to the reliability limiting mechanisms occurred.

An unfortunate consequence of this geometry problem is that with the poor yield of 2.0μm SEC chips there will be a relatively small sample size for the life test. The plan was to have 100 SEC chips from each fabricator under each stress condition in the life test. However, these yield results actually worked to our benefit. We had a larger number of Vendor A fabricated SEC devices to test, so we would have a better chance of seeing failures in devices that appear to have high reliability, based upon the wafer level reliability test results.

B. Package Yield Test Results:

Post package yield test results do not indicate any failures that are related to WLR tested mechanisms. The package yield failures were clearly packaging related mechanical faults. A small number of chips were functional, but failed the package leak tests. The net reduction in usable SEC devices was insignificant. Total yields were: Vendor A 462; Vendor B 120; Vendor C 102. Yielded packaged chips were installed in boards for testing. Table 4 shows the distribution of vendor chips in the life test setup.

Table 4: Yielded SEC Chips

	Oven Boards @ 175°, 5.0V	Room Temperature @V_{DD}=7.0 V.
Vendor A	189	189
Vendor B	60	60
Vendor C	51	51
Total Chips	300	300

C. Correlation of Yield with WLR Test Results Discussion:

As indicated above, there is significant correlation between the TDDB results that suggest a gate oxide defect tail and the relatively low yield of Vendor C and Vendor B SEC chips. Vendor A chips have excellent gate oxide quality indications both from the TDDB results and relatively good SEC yield. Since the number of chips involved in this correlation is statistically significant, it is reasonable to assume that there is correlation between chip yield and gate oxide quality, as measured at the wafer level with the voltage ramp test. We could not find any correlation between the other wafer level measured parameters and parametric, reliability, or chip yield data.

VI. Life Test Hardware Configuration:

The life test defined for this task is divided into two general environments: 1) Oven based at 175°C with the power supply voltage set at 5.0 Volts and 5.0MHz clock drive to the array. 2) Room temperature (23°C) with the power supply voltage set at 7.0 Volts and 5.0MHz clock drive to the array. Each test environment is designed to emphasize specific failure mechanisms of those tested with the WLR test structures, while running the SEC chips at a clock frequency (5.0MHz) that will cause the chips to draw significant power supply current. Three hundred SEC chips were used in each environment, with the yielded SEC population equally divided between the two test environments. All yielded SEC packages from Vendor B and Vendor C were used. Vendor A SEC packages were used to fill the remainder of the 300 chip capacity of the test fixtures.

Twenty test boards containing 30 test sockets per board and a temperature rating of 175°C were purchased for the life test. An aluminum shelf assembly was constructed to secure the boards inside the test oven. The shelf system holds 10 test boards (300 chips) in an orientation such that the circulating air flows between the boards to reduce any temperature differences between chips. An identical set of boards were placed on a table to operate at room temperature.

Each test board is wired to a small rack (schematic diagram in Figure 6) that contains two power supplies and a clock driver board. The cabling to the test boards contain power, ground, self-oscillate enable, and the external clock (5.0MHz). The cabling is routed individually from each board to the power rack, so that there can be no cross talk between boards due to cross-talk in a ground loop. The power rack has a single point connection for power and ground. The clock to each board is buffered individually using a source matched clock driver chip to reduce the possibility of clock ringing.

Once the life test had begun there were pre-defined intervals at which the oven in the test system was returned to room temperature to test the chips in self-oscillate mode. Test intervals were at one week (168 hours), two weeks (336 hours), four weeks (672 hours), eight weeks (1344 hours) and the final test at sixteen weeks (2688 hours of total operating time). The primary purpose for these tests was to be able to estimate the time of failure of any chips that failed.

VII. Life Test Results:

Periodic checks on the number of failures that occurred during the life test produced some interesting results. At some point between the first two test intervals, most of the fall-outs, in the devices that were fabricated in the wafer lots which showed high gate oxide defect density occurred. The majority of these failures occurred in the room temperature test boards operating with the 7.0 Volt power supply. A summary of the post life test data is contained in Table 5.

Table 5. Post Life Test Fraction Functional Data

	Lot A Vendor A	Lot B Vendor A	Lot C Vendor A	Lot E (HA) Vendor B	Lot F (HA) Vendor B	Lot D (JA) Vendor C	Lot D (JB) Vendor C
Oven @175°C	60/60	96/96	58/60	0/24	5/30	1/6	12/24
Room @23°C	41/41	85/85	84/84	0/22	9/20	0/4	3/44

Failures on the room temperature board were grouped in lots more or less in direct relationship with the oxide quality. Chips from the Lot E and Lot F were the first chips to fail. By week four, the majority of the chips from Lot D had failed and all chips from Lot E had failed. Some time before the week eight test, essentially all Lot D chips that were going to fail had failed (a few failed after week eight) for a final survivor count of 3 out of 48. In contrast, chips from Lot A, Lot B and Lot C had no failures at the end of the entire sixteen week test.

Chips on the oven mounted boards, operating at 175°C and 5.0 Volts, had similar failure characteristics at the sample intervals. The time to fail was longer, but by the end of the sixteenth week all of the chips from Lot E had failed, and only 9 out of 20 from Lot F survived. Chips from Lot D fared somewhat better with 11 survivors out of 30 chips. At the end of sixteen weeks only one chip from Lot A had failed and there was 100% survivors from Lot B and Lot C.

This data clearly shows that, based upon wafer level assessments indicating high gate oxide defect density in three of the wafer lots, there is a high failure rate in the life test. The higher stress voltage at room temperature accelerated failures at room temperature as indicated by early failures, above. Oxide test data showing no defect tail for the designed area of the TDDB test capacitor in Lot A, Lot B and Lot C also show a very low failure rate. However, providing hard data to prove that the failures observed were indeed oxide breakdown caused was more difficult than we expected.

None of the frequency of self oscillation data provided an indication of transistor parameter degradation that could be attributed to hot carrier damage. We did not expect to see any hard failure to occur due to hot carrier damage, but we had assumed that if hot carrier damage did occur it would show up as a frequency change. Since no statistically significant frequency changes could be detected, it is assumed that there was no significant hot carrier damage present.

The chips in the oven would have been at a temperature high enough to anneal out hot carrier damage as rapidly as it occurred. Chips operating at 7.0 Volts would have been most susceptible to hot carrier damage, but since the power dissipation from operating the chips at 5.0MHz with high supply voltage resulted in chips operating at package temperature over 100°C, it is likely that if any hot carrier damage occurred, it too would have been annealed out. Since we saw no

significant lot to lot variation in wafer level hot carrier damage susceptibility, we did not really expect to see any correlatable results from the life test.

VIII. Failure Analysis

The goal of the failure analysis was to provide hard evidence that a failure had occurred at a specific location in the SEC chips experiencing functional failure and to provide a reasonable accurate assessment of the failure mechanism that was responsible. We expected that since most of the early failures occurred in the high supply voltage samples, we should be able to find oxide breakdown on the failed chips. Given the number of failures (146 total from both test fixtures) that occurred and our limited budget for failure analysis, we were able to only sample the failed population.

The first step in the failure analysis process was to examine the test data to determine if there was an isolated failure in the array. We found that there were no cases where the failure was isolated, in fact the failure test results appeared to indicate that the failure involved the whole chip. In general, the majority of the failures had the property that the power supply current was either very small (low microampere range) or very large, with most chips operating at the low microampere range. Since nothing conclusive could be deduced from the interface pins, we selected 78 chips to be sent for lid removal. The majority of the chips selected were taken from the room temperature, 7.0 Volt V_{DD} samples.

After lid removal, the first task was to inspect the chips at low magnification. The most startling observation was that in all cases where the device exhibited low supply current, the bond wire to V_{DD} or Ground was fused. There were 33 out of 42 from the room temperature test group and 19 out of 36 from the oven test group that showed fused bond wires. The low supply current observation was related to the fact that current was flowing through the input pins (via the pad protection circuits) to power up the chip. All of the remaining chips showed evidence of heat damage to the power or ground bond wires, suggesting that a rather large amount of current had passed through the wire. This observation strongly suggests that the bond wire failures were caused by latch-up.

Gate oxide failure caused latch-up is a logical explanation of this high incidence of bond wire failures. If one thinks about what happens when a gate oxide failure occurs, in an N-channel transistor of an inverter in a p-well process, it is possible to describe the gate to substrate connection as the trigger input to the latch-up SCR (Silicon Controlled Rectifier). Figure 7 contains a diagram of a CMOS inverter substrate cross section, with an overlay of the latch-up bipolar transistors showing parasitic resistors from the MOS transistor channel region to the bipolar transistor base connections. Referring to Figure 7, when the N-channel transistor gate oxide breaks down and connects the gate to the channel, and when the gate potential is a logical "1" (5.0 Volts), the current is supplied to the base of the vertical NPN transistor of the latch-up pair in the inverter. As a result, latch-up will occur as soon as the input is a logical "1". A similar

scenario applies to a gate oxide failure in the P-channel transistor, with latch-up trigger occurring with the input at a logical "0".

To verify this explanation, we probed inside the packages of chips with failed bond wires to bypass the broken bond wires and supply power to the chips. The input pins were all tied to either V_{DD} or ground and the output pins were either open or connected to an oscilloscope. The array input pins were logically configured an for externally driven array clock with the clock pin connected to a triggerable signal source. The power supply voltage was ramped up very slowly to avoid any possibility of latch-up occurring by displacement of charge at power on. Of the 10 chips that we sampled in this manner, we observed that most of the chips would latch-up either immediately after the power supply voltage reached two or three Volts, while the remaining chips would latch-up as soon as the array input was toggled. It was not possible to address the array cell or cells that had the gate oxide failure without causing latch-up, so we were unable to narrow a search with a SEM to view the failed gate.

Closer visual examination (at about 350X) revealed some electromigration damage had resulted from the large latch-up current when the chip failed because of gate oxide breakdown. Even though this latch-up current caused electromigration is not valid as a use condition electromigration sensitivity assessment, it is interesting to see the degree to which each wafer lot was resistant to electromigration damage. There were only two chip failures in the Vendor A lots, and both failures were of the type that we assume are oxide failure caused latch-up, but there was no evidence of electromigration damage on these chips. The remaining chips, which were from Vendor B and Vendor C, were found to have varying amounts of electromigration damage. In general, we found a large number of hillocks on the Vendor B chip lots and relatively few hillocks on the Vendor C chip lots. This observation agrees with the WLR SWEAT test results which show that Vendor B lots have much less electromigration damage resistance than either Vendor C or Vendor A and the Vendor A lots that most are consistent.

The failed chips are in storage and may be analyzed some time in the future.

IX. Observations and Conclusions.

The correlation of WLR test results with life test results over a diverse range of fabricators was the goal of this work. Even though there was a significant number of failures of SEC devices during the life test, we are not able to find correlation between WLR hot carrier test results and functional device experience. This lack of observable correlation neither confirms nor rejects the validity of the wafer level hot carrier damage testing. It means that more controlled testing is needed because wafer level hot carrier tests on the particular wafer lots used in this study show approximately equal hot carrier damage resistance. A more meaningful test would require wafer lots that show varying degrees of hot carrier damage susceptibility based upon several wafer level hot carrier test methods.

The use of 1.6μm and 2.0μm channel length devices in this task contributed to reduced hot carrier damage observations. However, since the SEC devices that were operated at room temperature were using a 7.0 Volt power supply, the hot carrier damage rate would have been measurable if the devices junction temperatures had been lower. Hot carrier damage was observed at room temperature using single test transistors (both 1.6μm and 2.0μm channel lengths) operated at V_{DD} = 7.0 Volts, although, damage rate was rather low. Unfortunately, in this task we apparently observed a higher anneal rate than hot carrier damage rate. From a practical standpoint, the choice of geometry in this research task were too large to produce a damage rate that would exceed anneal rate at the junction temperatures that we experienced.

Results of this task clearly show correlation between TDDB test results and functional device yield and life test failure rate. However, the gate oxide quality ranged over a very wide spread of breakdown distributions. There is a high level of confidence that for this range of gate oxide defect distributions the WLR test results will detect wafer lots with high oxide failure rates. However, it is not clear to what degree less dramatic gate oxide defect density differences are correlatable with WLR tests.

We observed in this study that the gate oxide test capacitor area was too small to detect the defect tail in the Vendor A wafer lots. Larger area test capacitors (or even larger numbers of capacitors per wafer) may not be practical with a limited production ASIC device. As a result, it is not clear if WLR testing is able to distinguish differences in defect density in a wafer fabrication line that has a nominally low defect density. It is clear that based upon the results of this task, that the WLR TDDB testing will detect a defect density disaster before ASIC devices are packaged and life tested.

Wafer level electromigration test results also show significant differences between the wafer lots used in this task. The three wafer fabricators ranged from very electromigration resistant to dangerously electromigration prone. There was sufficient indication that some of the wafer lots probably would be rejected for high reliability applications. Unfortunately, because of the gate oxide breakdown caused latch-up, there was no data to show that under the conditions of these life tests, there was a measurable electromigration damage rate difference between the wafer lots. It is not possible to separate evidence of hillock growth due to electromigration under the life test conditions from the hillock growth caused by the latch-up current flow.

On the more positive side, given that the actual latch-up current density is unknown, there is clear correlation in the results indicating that WLR electromigration test results predicted the hillock growth likelihood on a lot to lot basis. The Vendor A lot had no hillock growth in the two oxide failure chips while the Vendor C lot showed a much lower hillock growth rate than the Vendor B lot. Vendor B and Vendor C both have similar metal composition. In SWEAT measurements, Vendor C has much smaller wafer to wafer variations in t_{50} than Vendor B. It remains for further correlation studies to show that these kinds of extreme differences in WLR electromigration test results will predict higher hillock growth rates in devices operated at

"normal" current density stress conditions in moderately high burn-in temperature conditions (such as 175°C).

Results of this correlation study are very encouraging. At the very least the WLR tests are a good disaster monitor. To further build confidence in WLR testing, it is recommended that a larger scale correlation study be conducted with ASIC devices intended for actual military use. A more conclusive study would need a larger ASIC sample size and an ASIC that has been designed using the best available "Design for Reliability CAD Tools". These ASIC devices should be fabricated in at least two different wafer fabrication sources and inserted into the wafer line at two or more randomly chosen times. The same kinds of WLR test methods used in this task would be used to identify any statistically significant differences between the wafer lots. The ASIC devices would then be placed into a moderately stressing burn-in test environment and operated for at least 4000 hours. If the sample size of ASIC chips used in this follow-on study is large enough, there should be a statistically significant number of failures to serve as a sound basis for comparing the WLR test results.

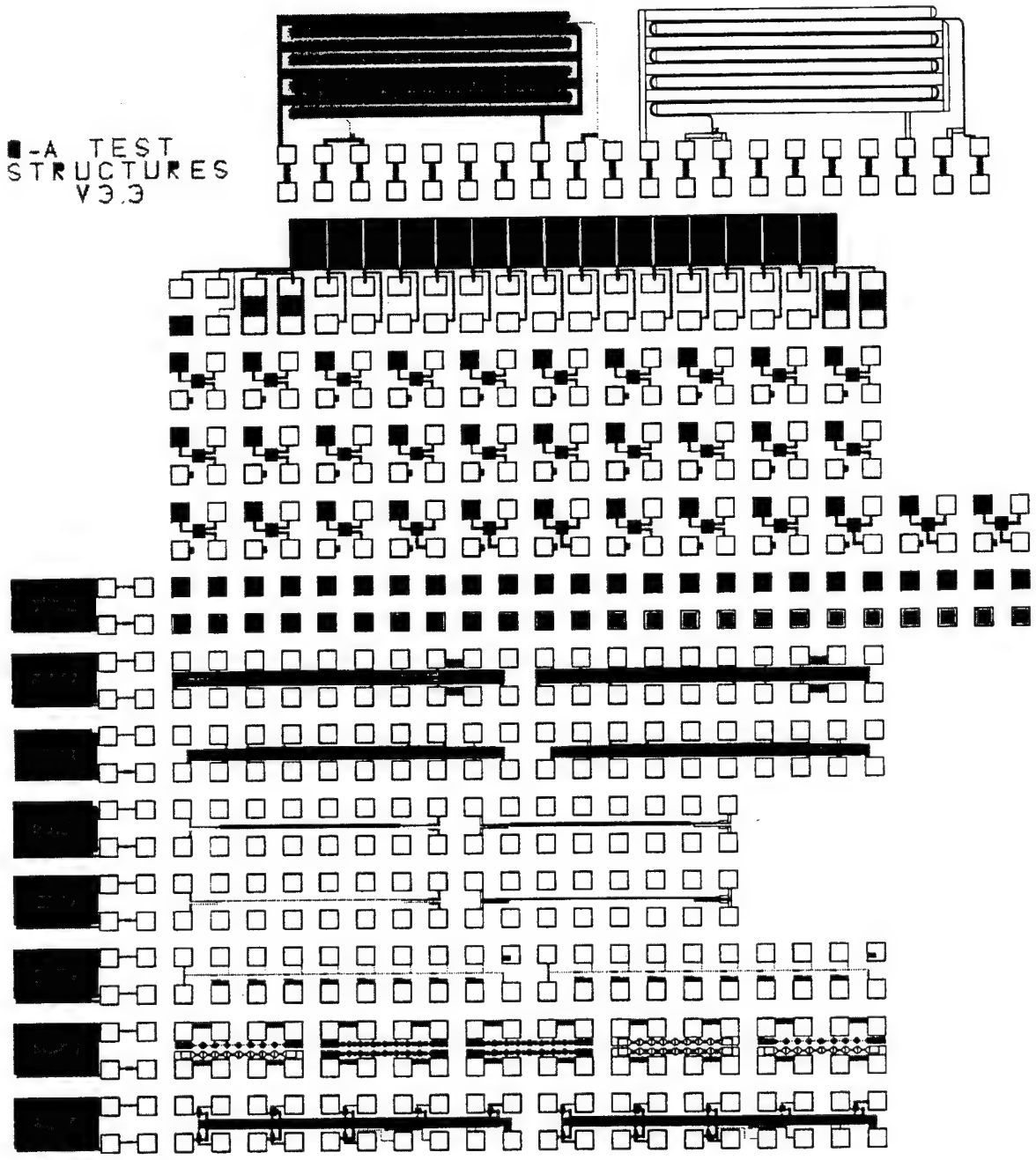

Figure 1: Wafer Level Reliability Test Chip Layout. Test structures used in this work are (relative to the bottom row): 1) Hot Carrier structures in rows 9,10, and 11. 2) SWEAT structures in row 2. 3) TDDB capacitors are in the left column.

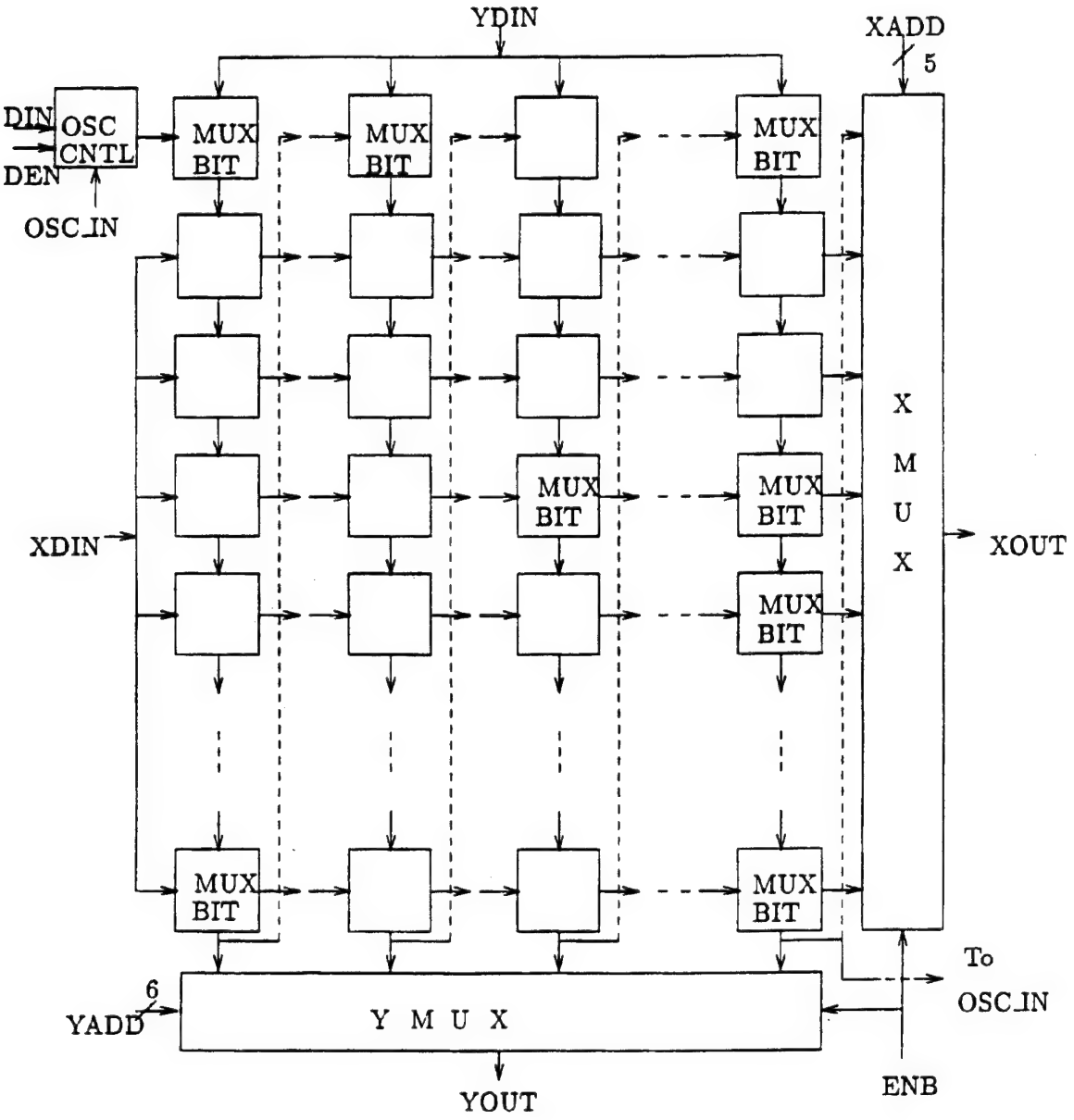

Figure 2: SEC Chip Functional Block Diagram. The SEC chip that was fabricated is a 64 X 22 array of MUX BIT cells.

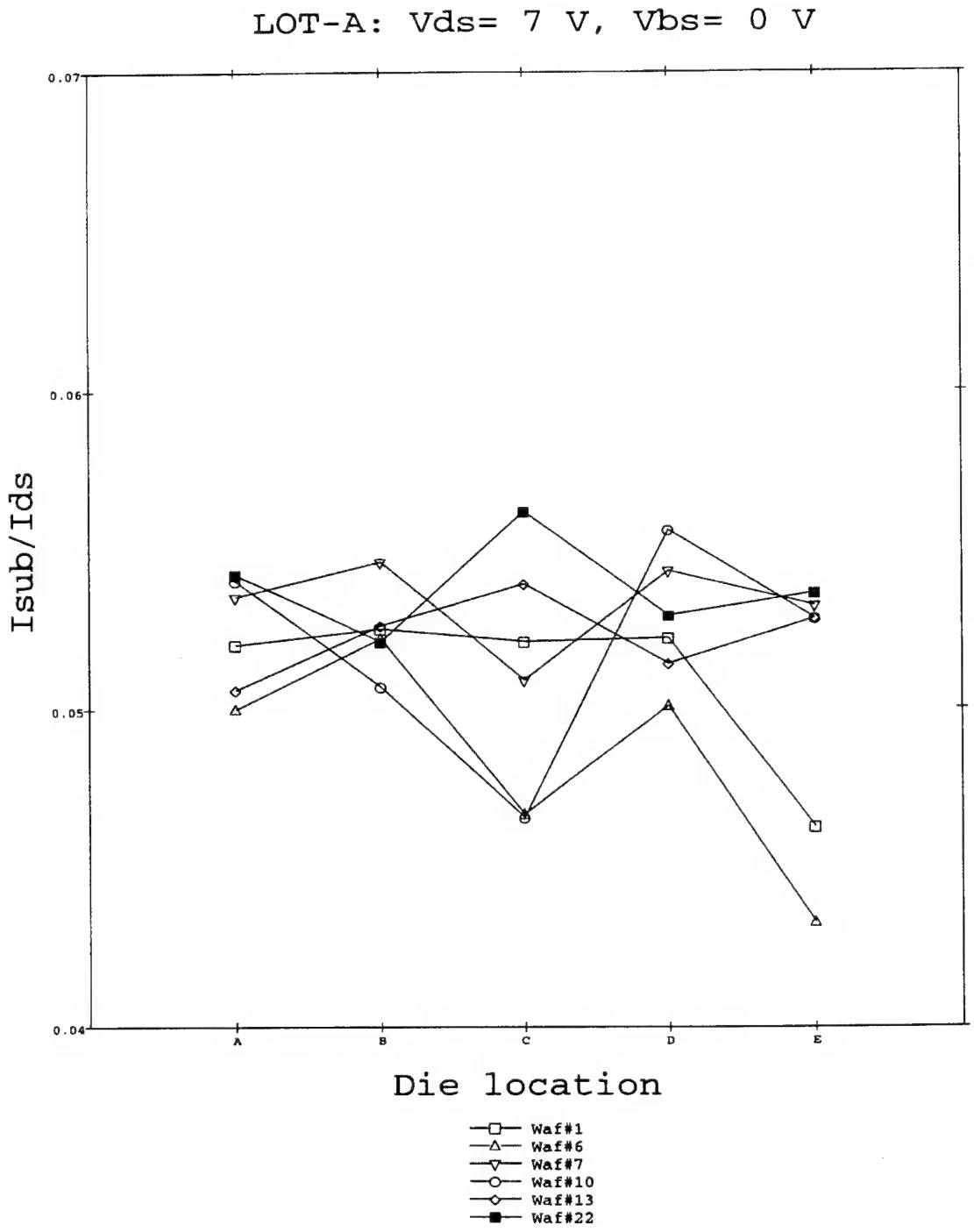

Figure 3a: Hot Carrier Test Data, Vendor A, Lot A.

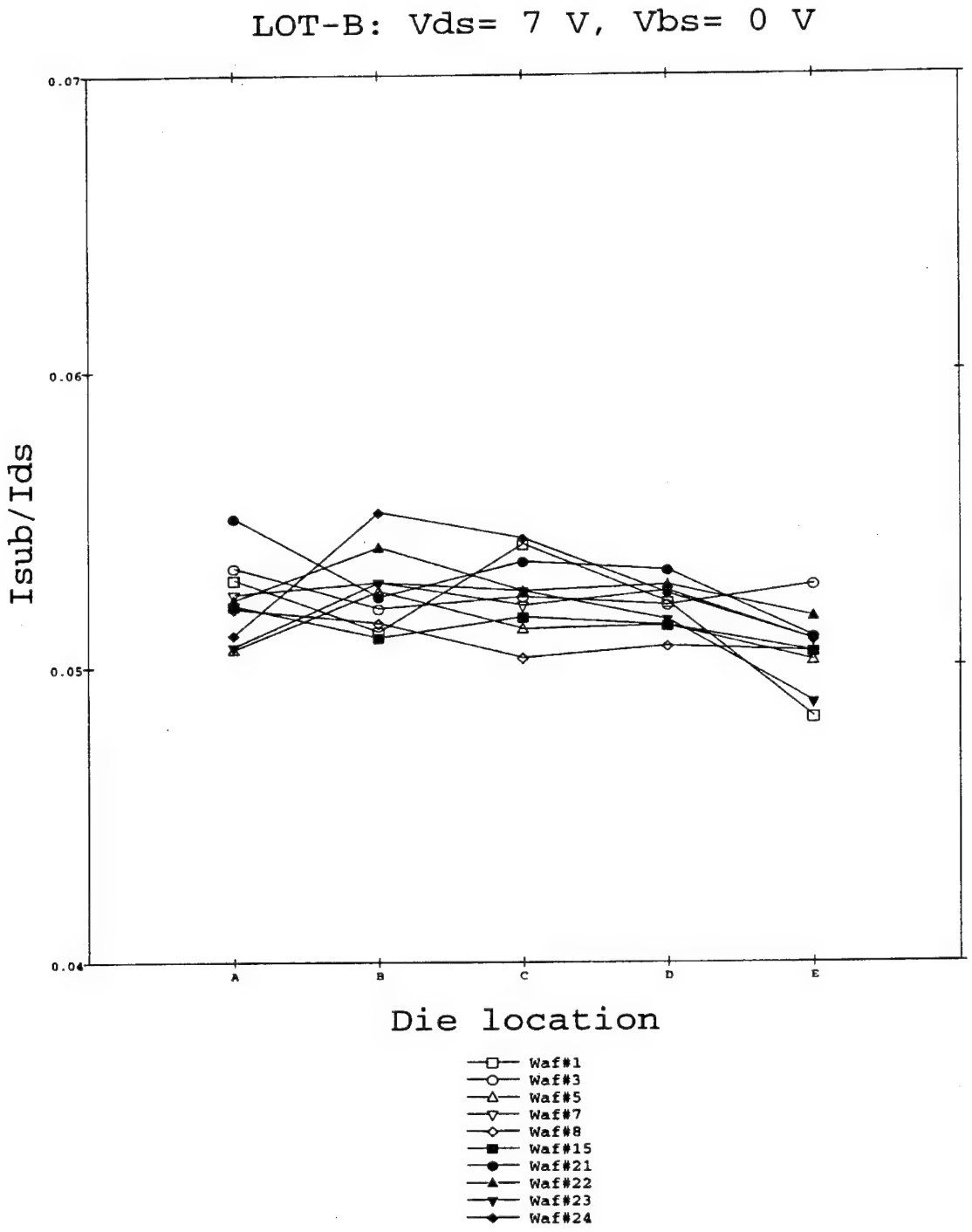

Figure 3b: Hot Carrier Test Data, Vendor A, Lot B.

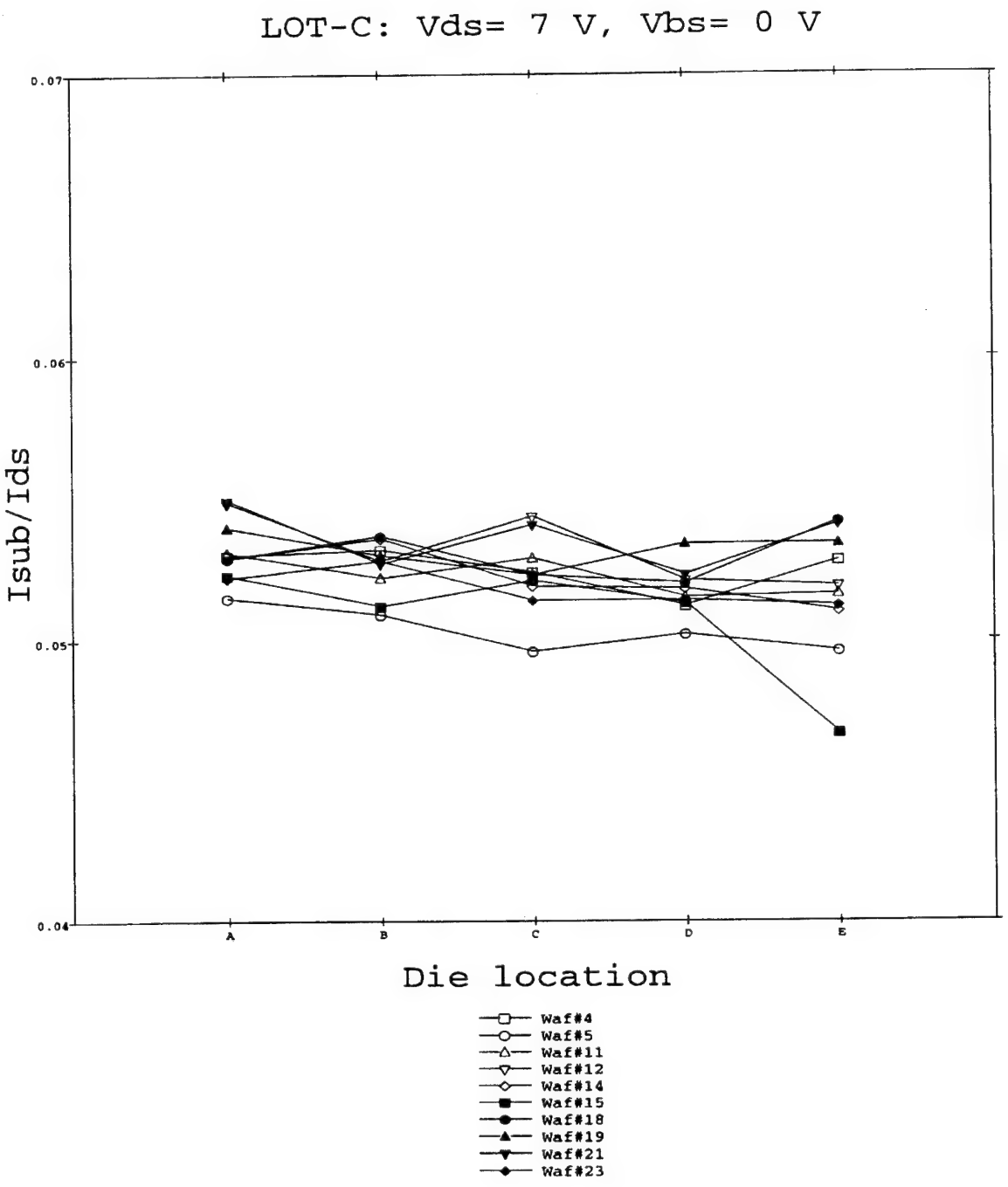

Figure 3c: Hot Carrier Test Data, Vendor A, Lot C.

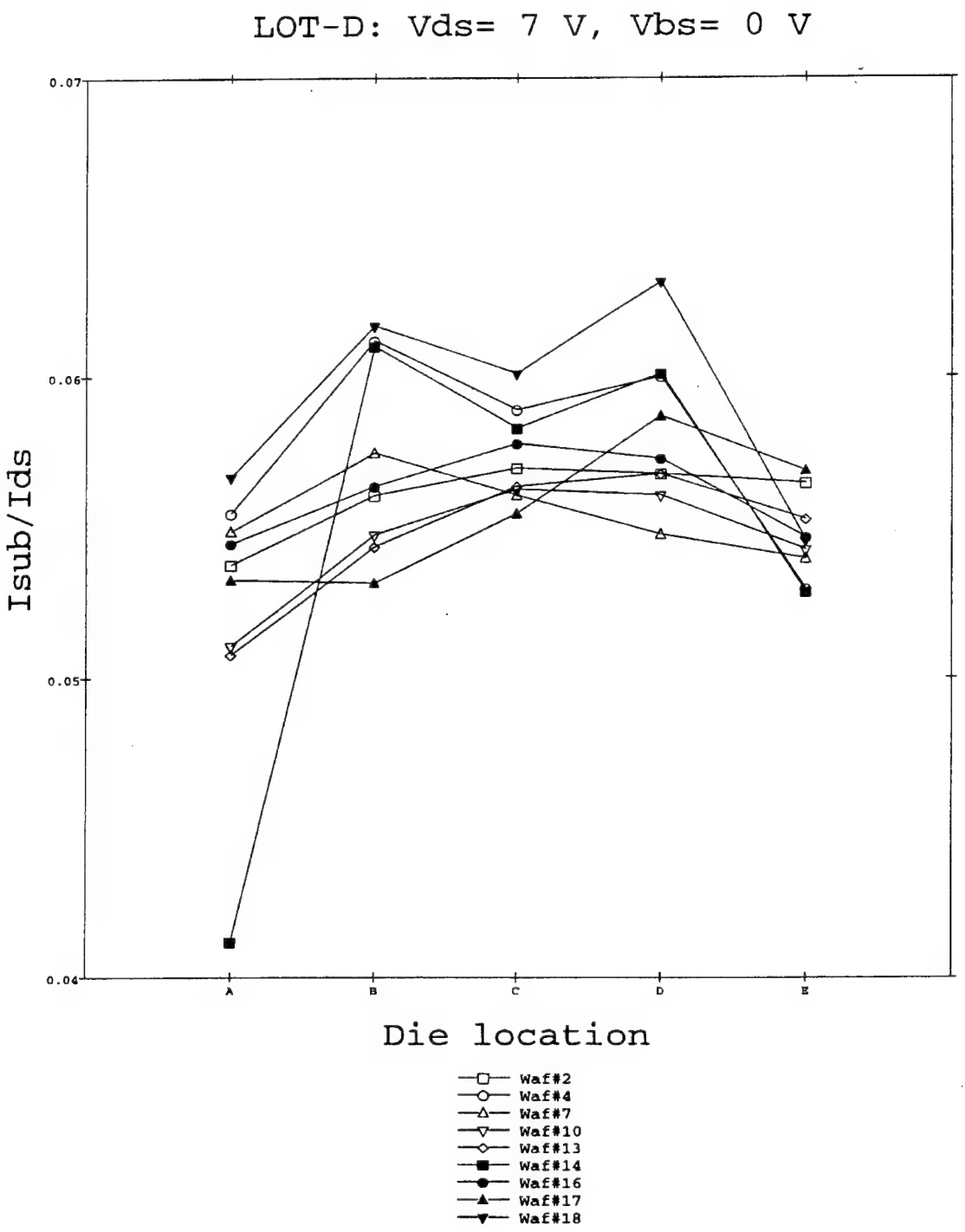

Figure 3d: Hot Carrier Test Data, Vendor C, Lot D.

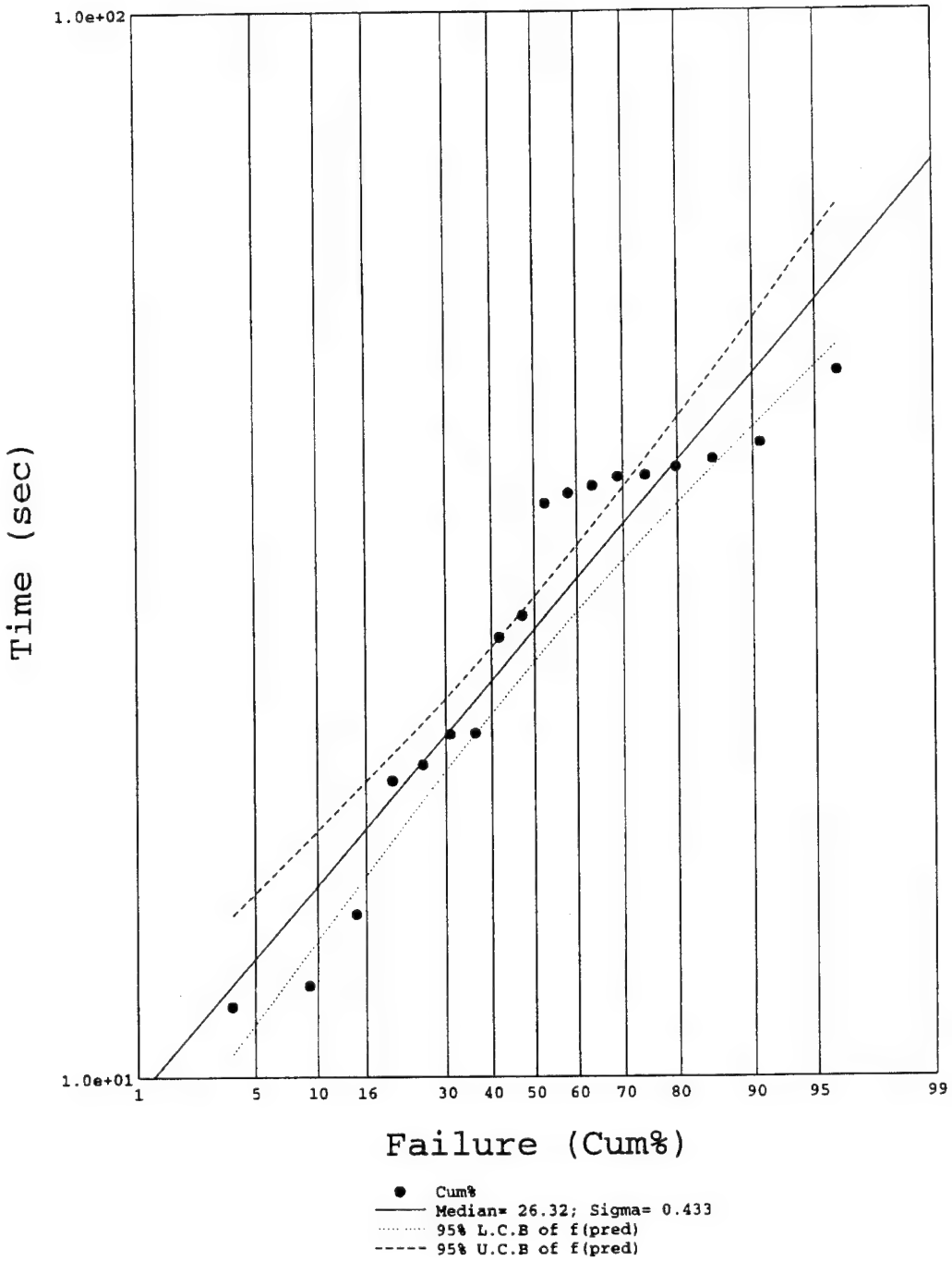

Figure 4a: SWEAT test results showing large lifetime variations- Lot F, Wafer No. 9. Approximately normal for the calibration used.

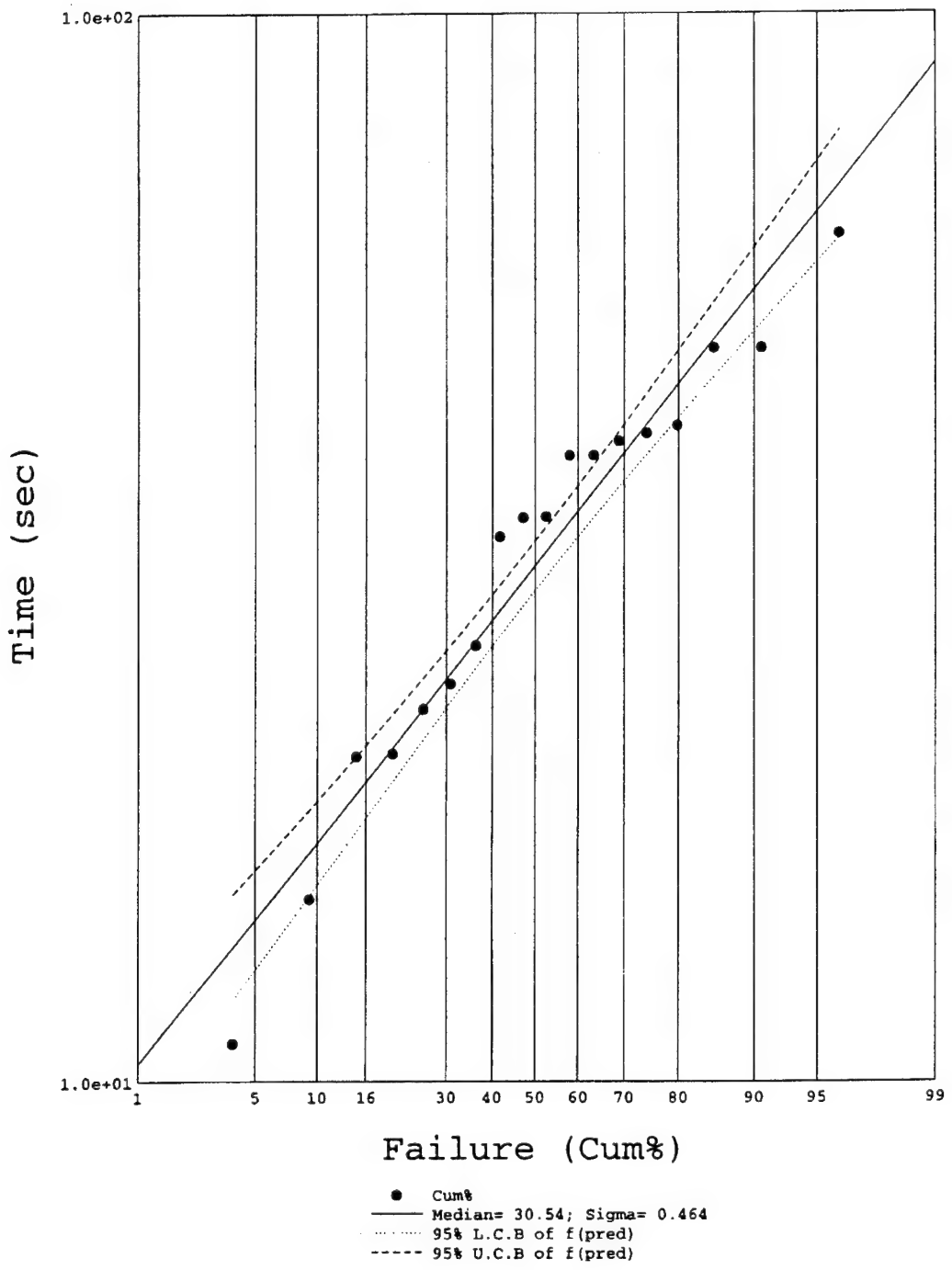

Figure 4b: SWEAT test results showing large lifetime variations- Lot F, Wafer No. 10. Approximately normal for the calibration used.

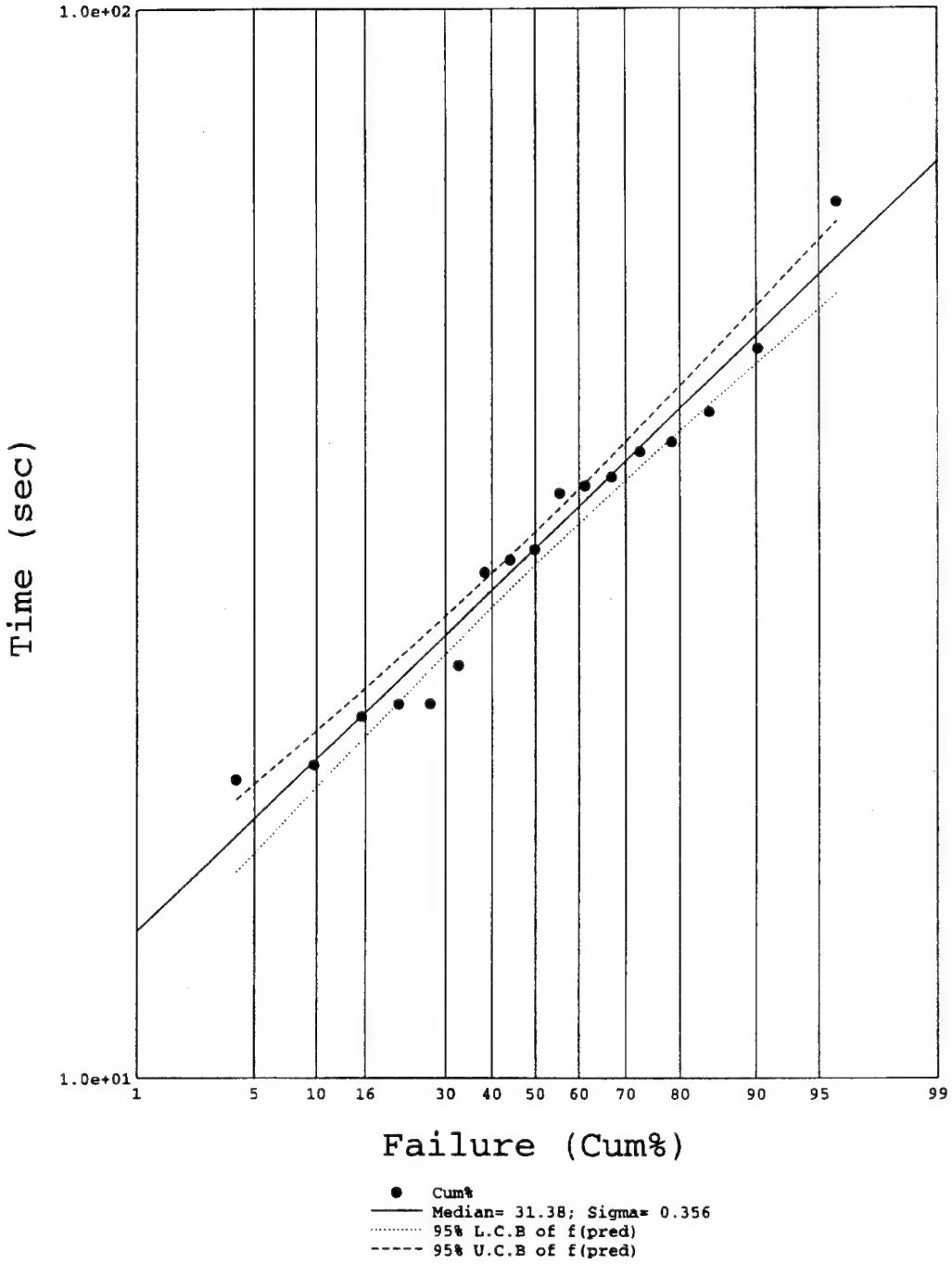

Figure 4c: SWEAT test results showing large lifetime variations- Lot F, Wafer No. 11. Approximately normal for the calibration used.

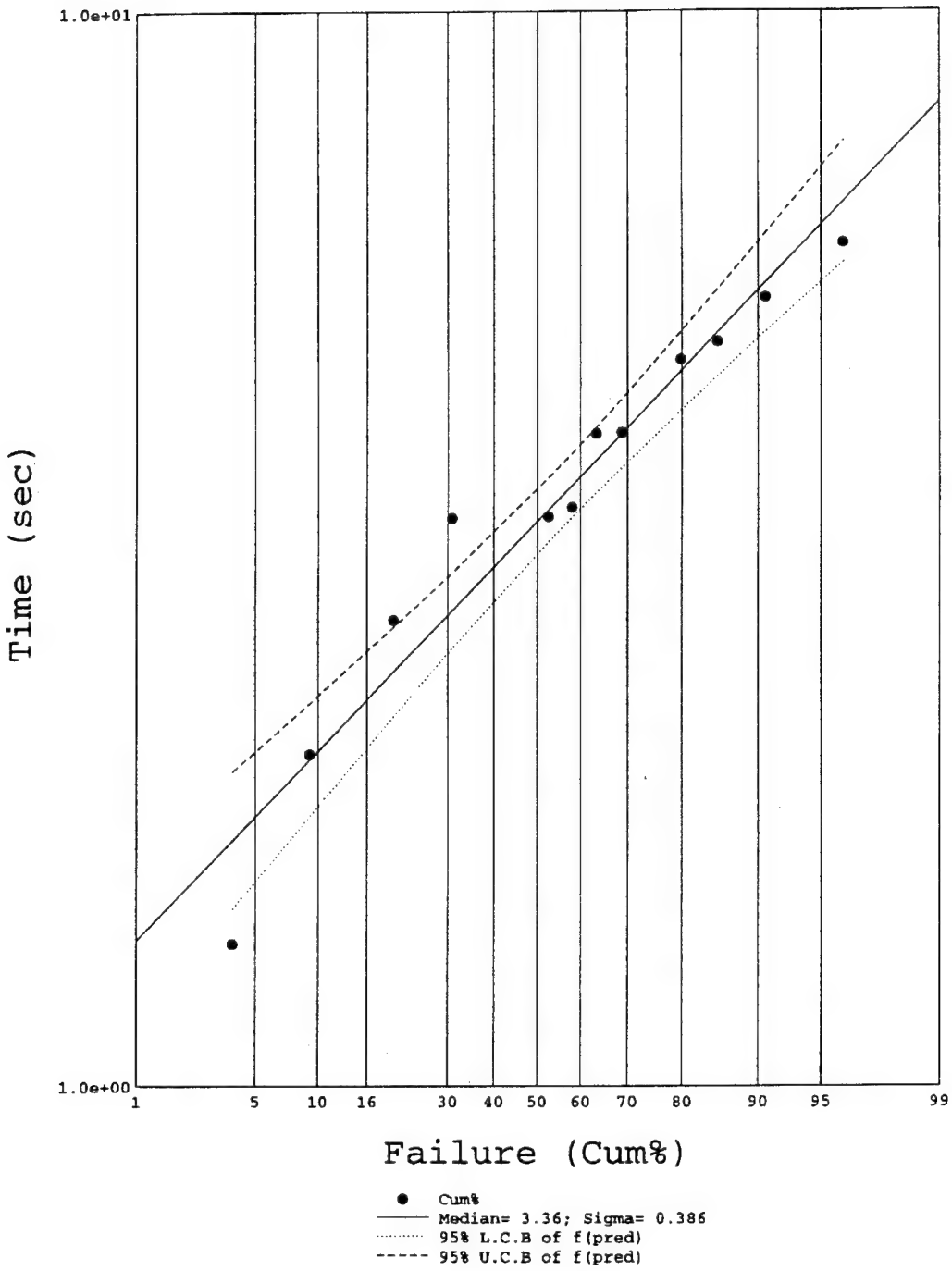

Figure 4d: SWEAT test results showing large lifetime variations- Lot F, Wafer No. 12. Extremely unusual variation from normal.

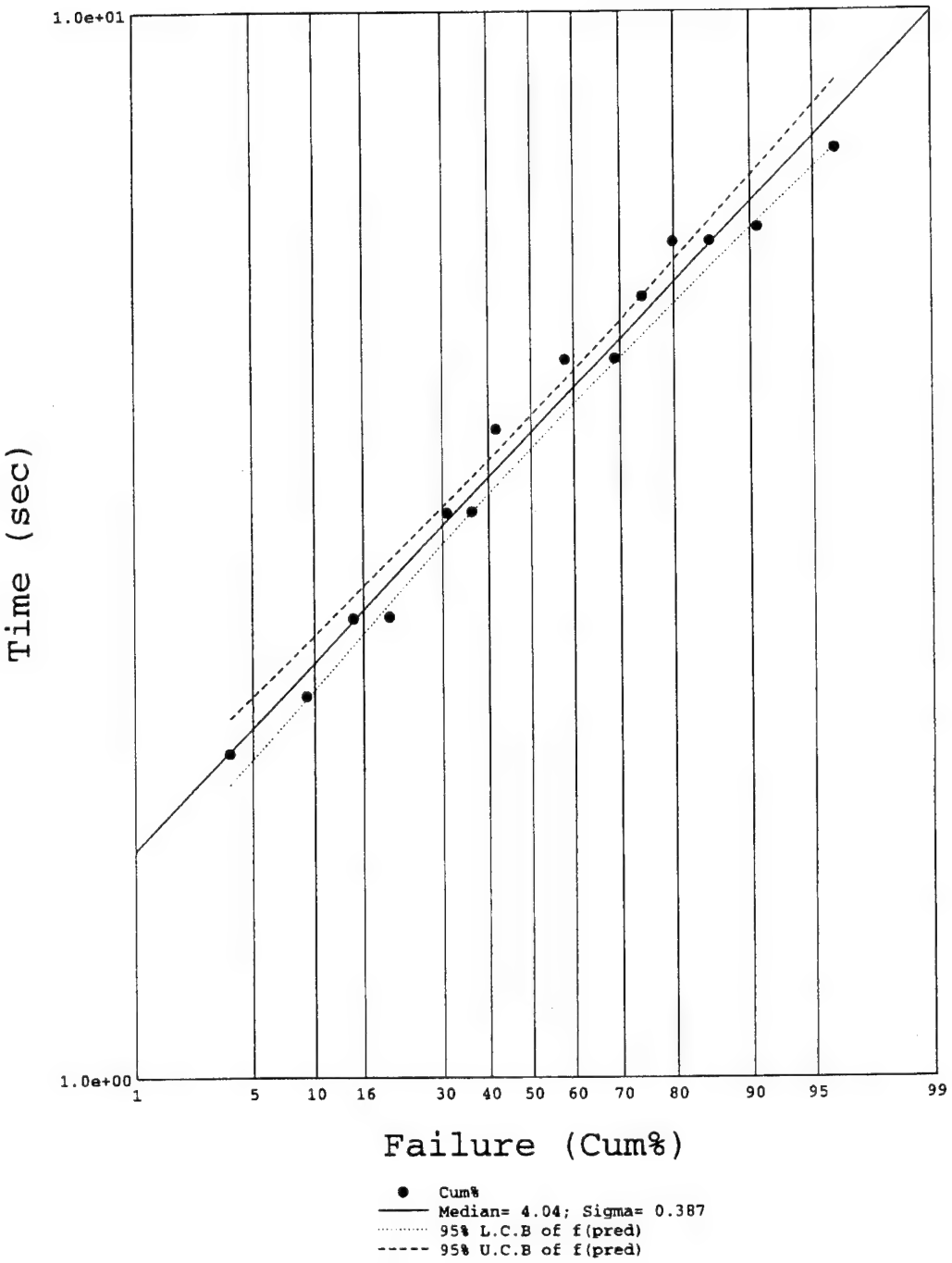

Figure 4e: SWEAT test results showing large lifetime variations- Lot F, Wafer No. 13. Extremely unusual variation from normal.

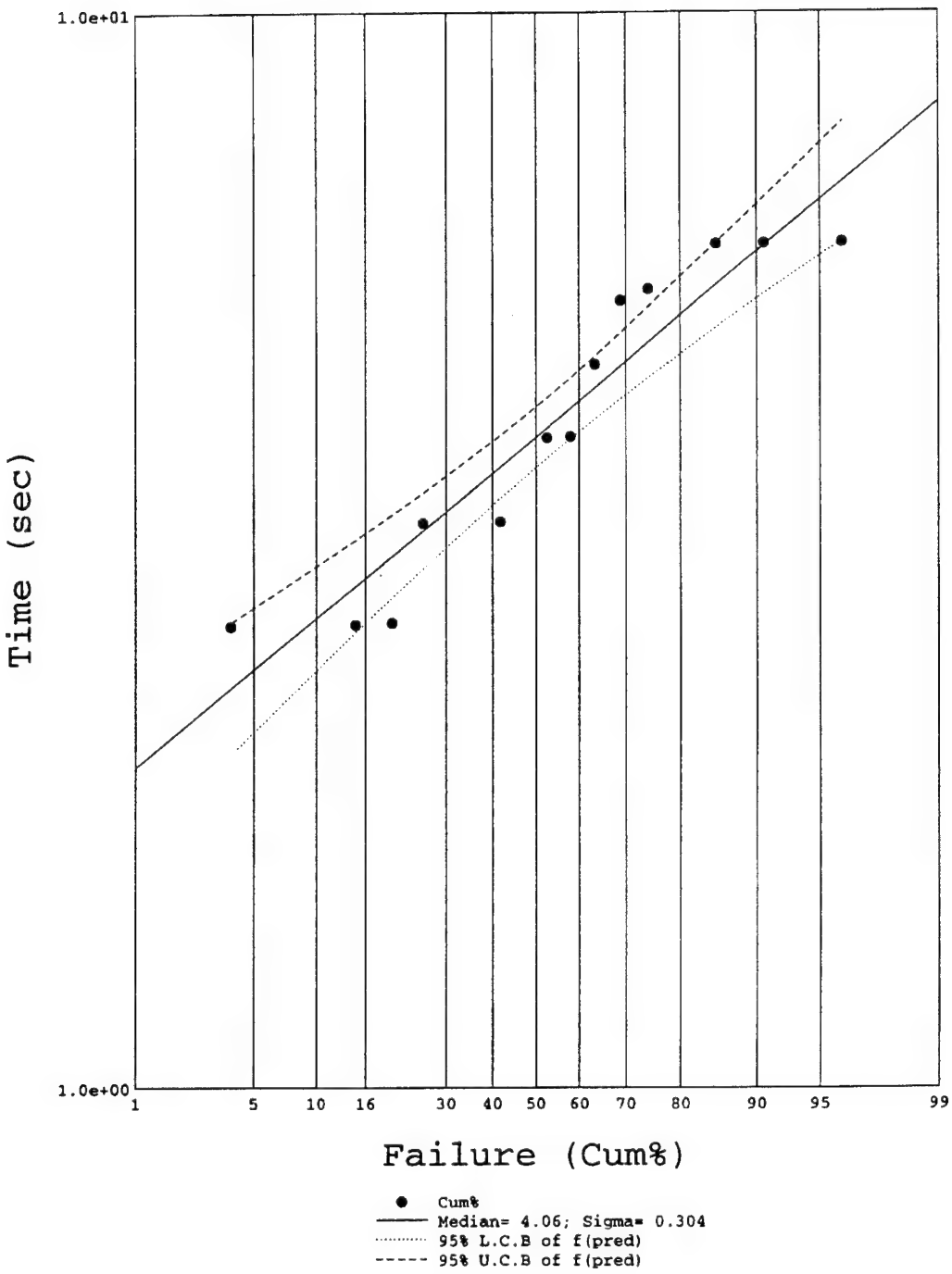

Figure 4f: SWEAT test results showing large lifetime variations- Lot F, Wafer No. 14. Extremely unusual variation from normal.

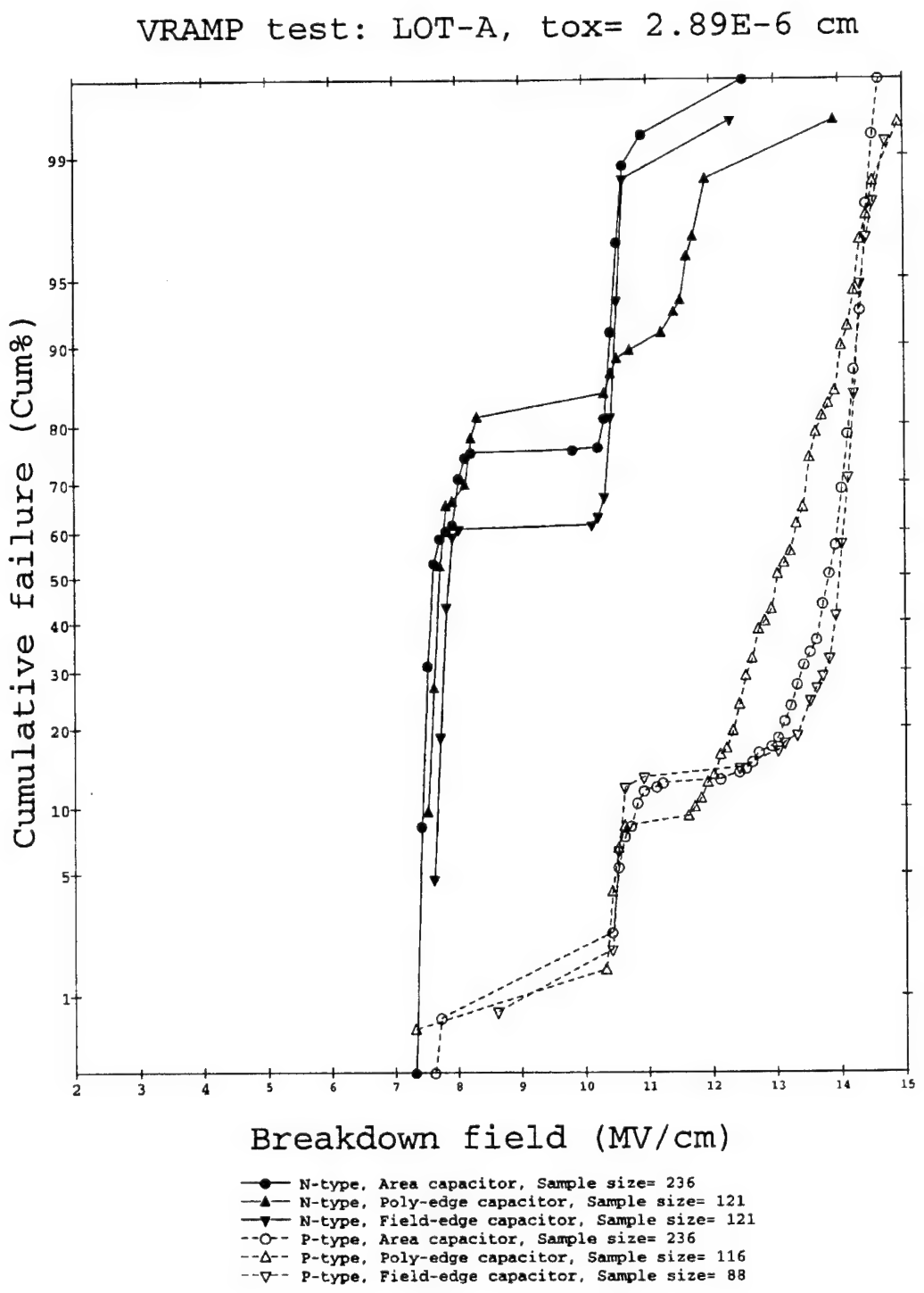

Figure 5a: Voltage Ramp TDDB test results- Lot A, Vendor A.

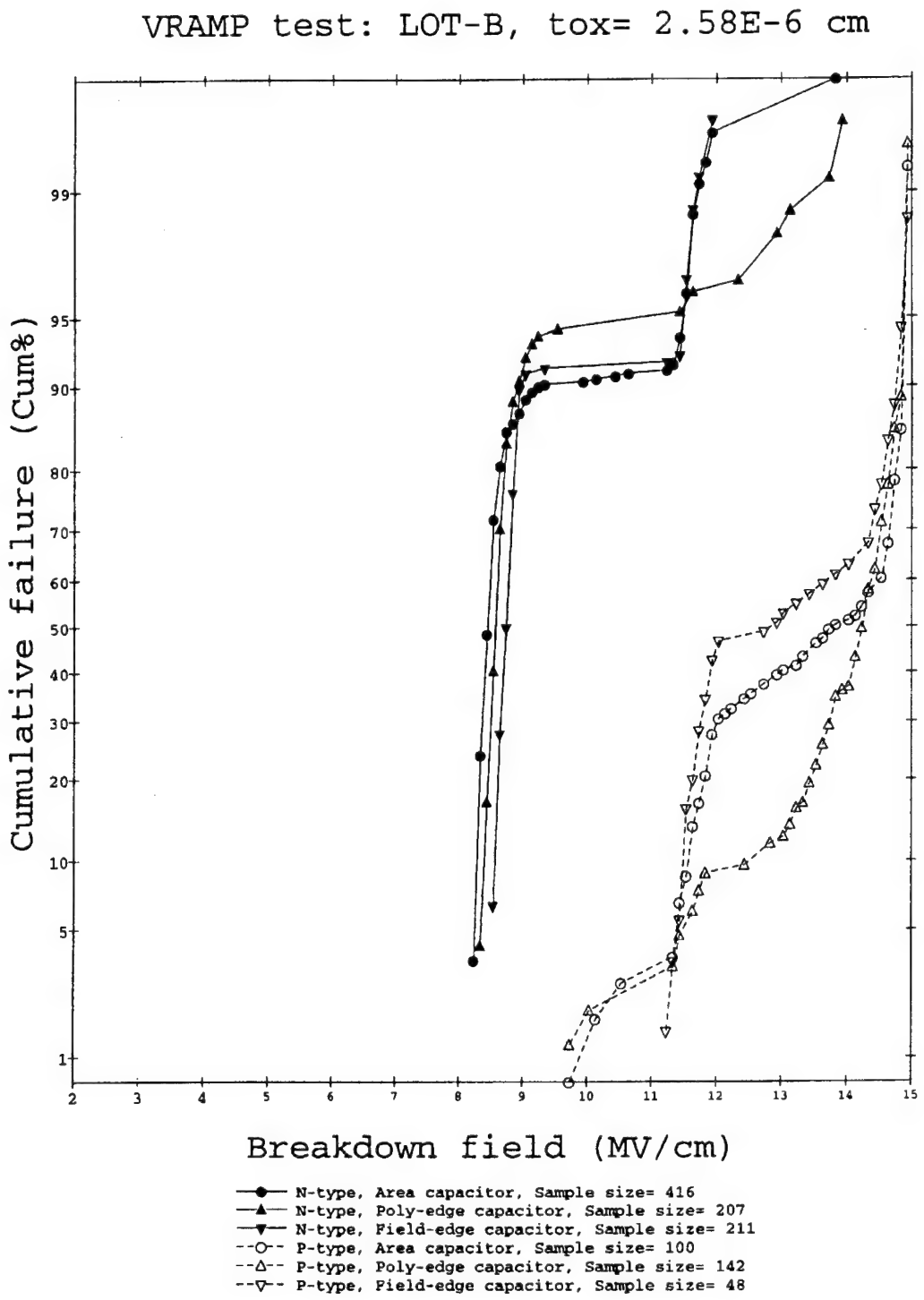

Figure 5b: Voltage Ramp TDDB test results- Lot B, Vendor A.

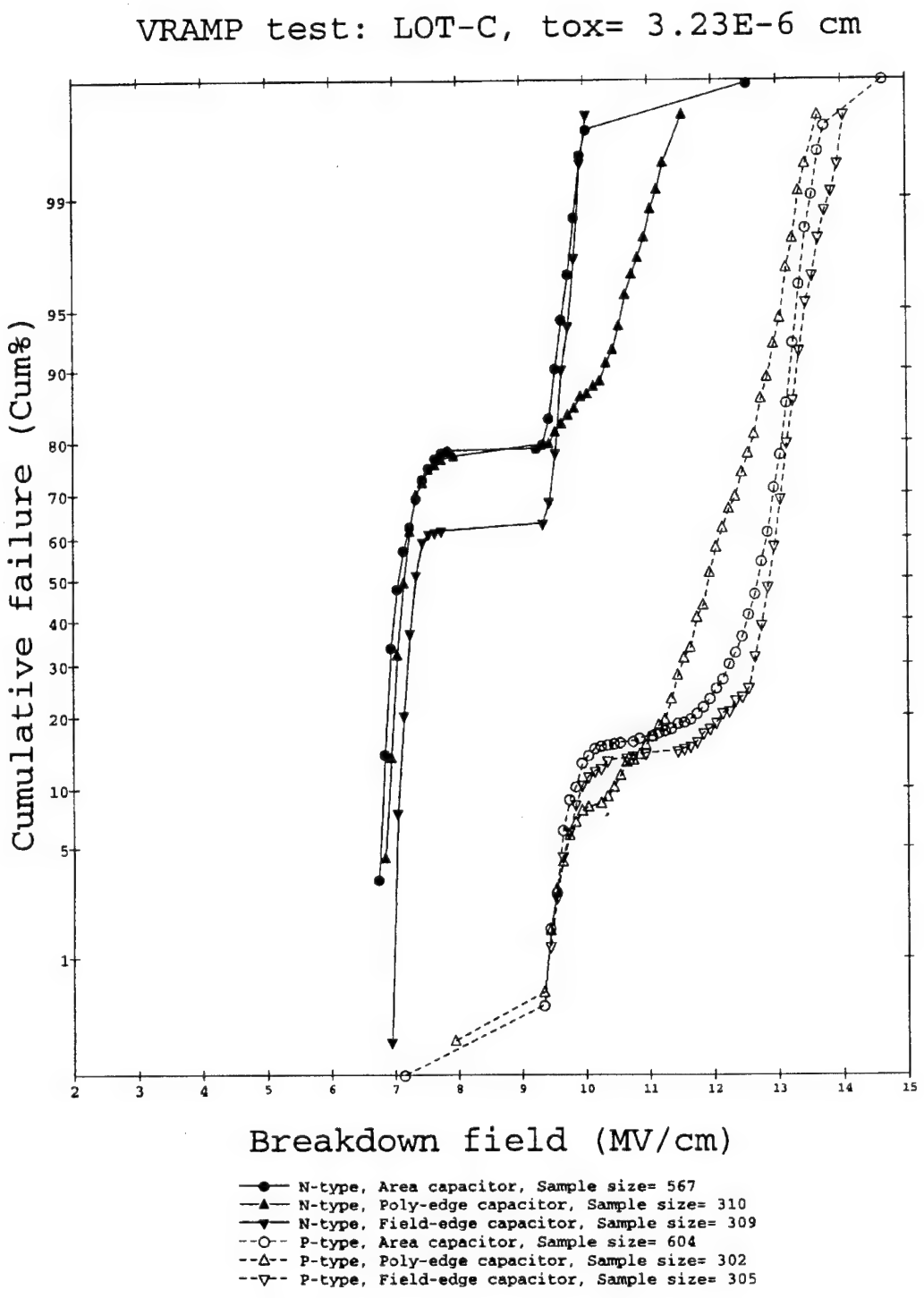

Figure 5c: Voltage Ramp TDDB test results- Lot C, Vendor A.

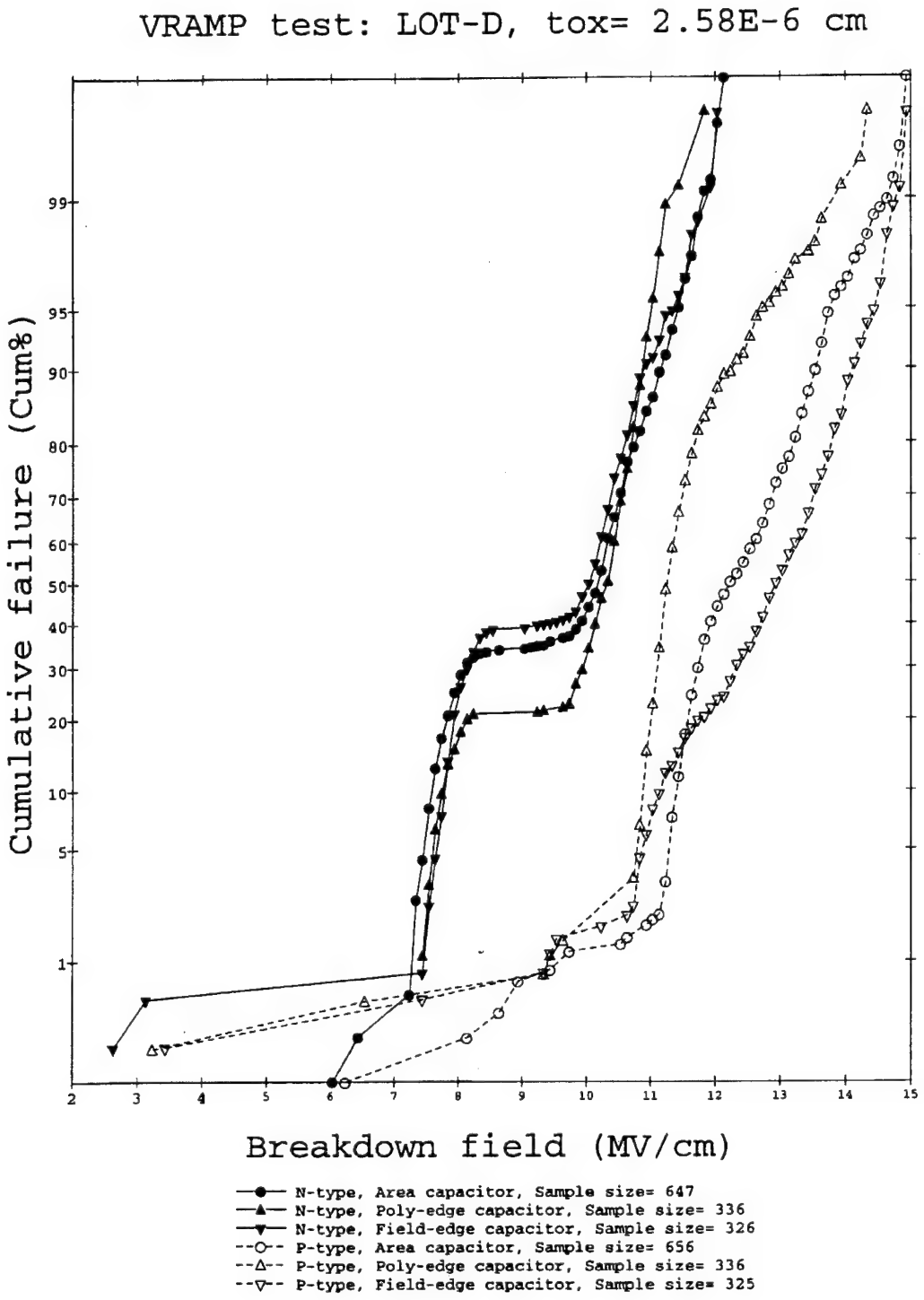

Figure 5d: Voltage Ramp TDDB test results- Lot D, Vendor C.

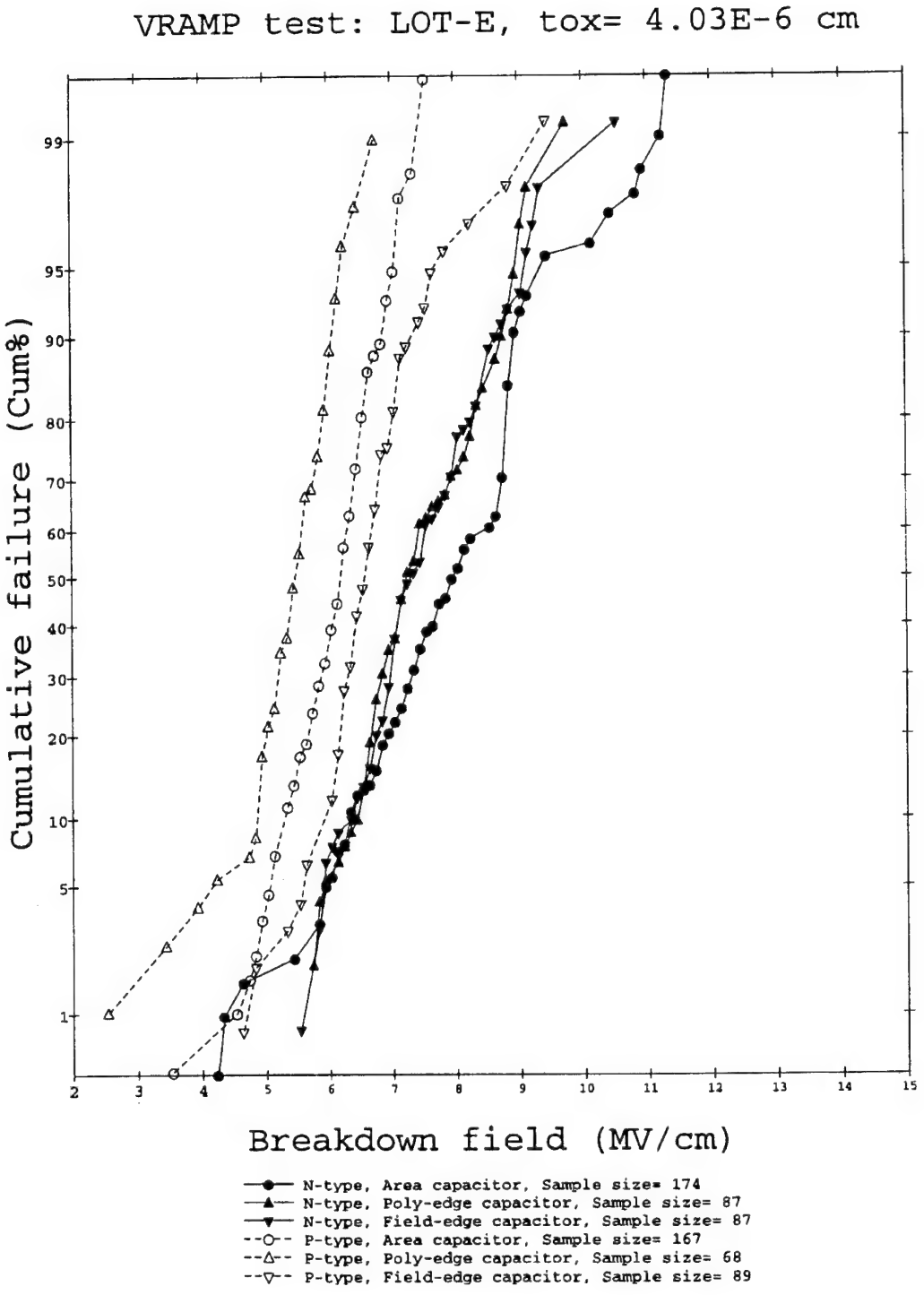

Figure 5e: Voltage Ramp TDDB test results- Lot E, Vendor B.

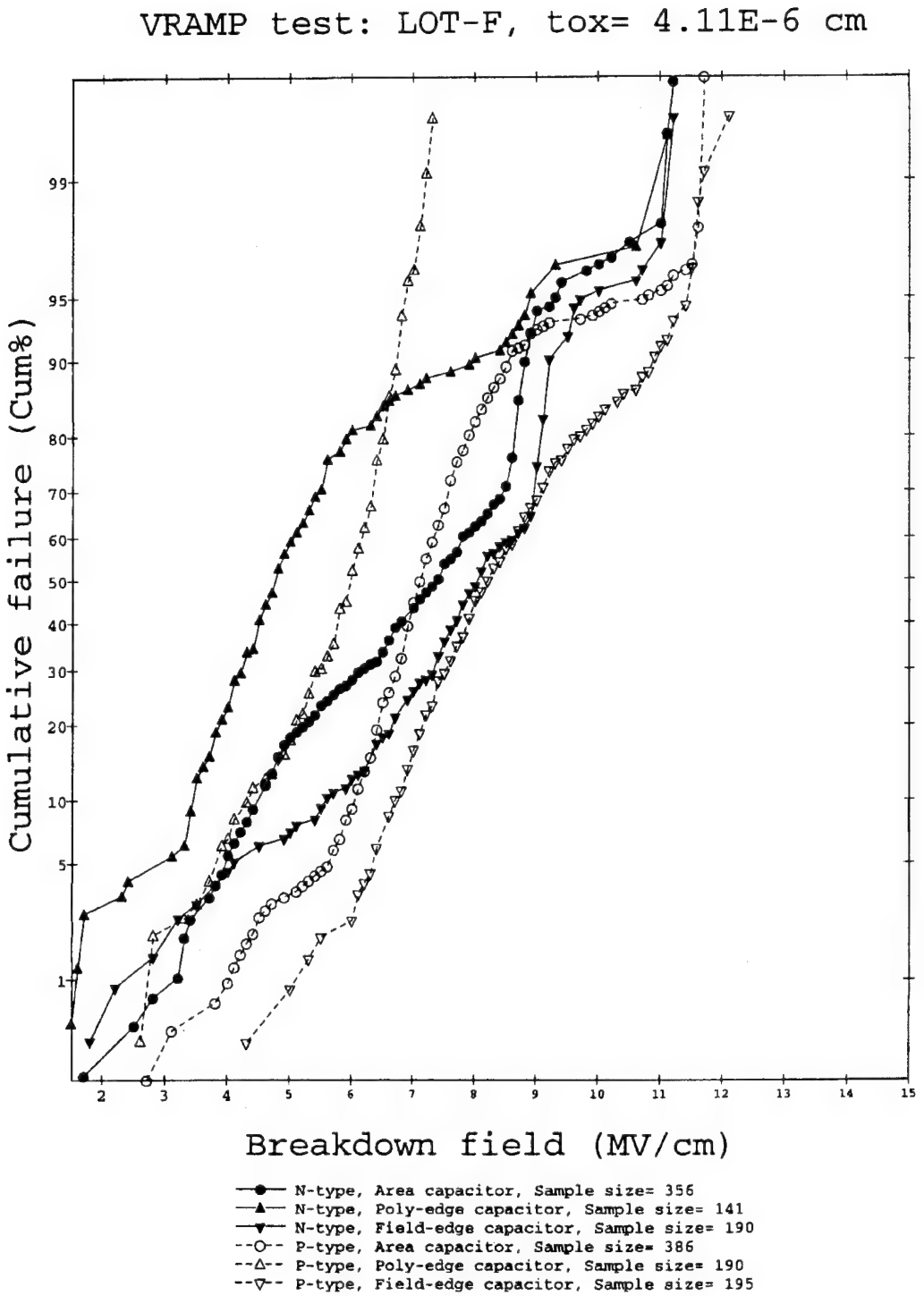

Figure 5f: Voltage Ramp TDDB test results- Lot F, Vendor B.

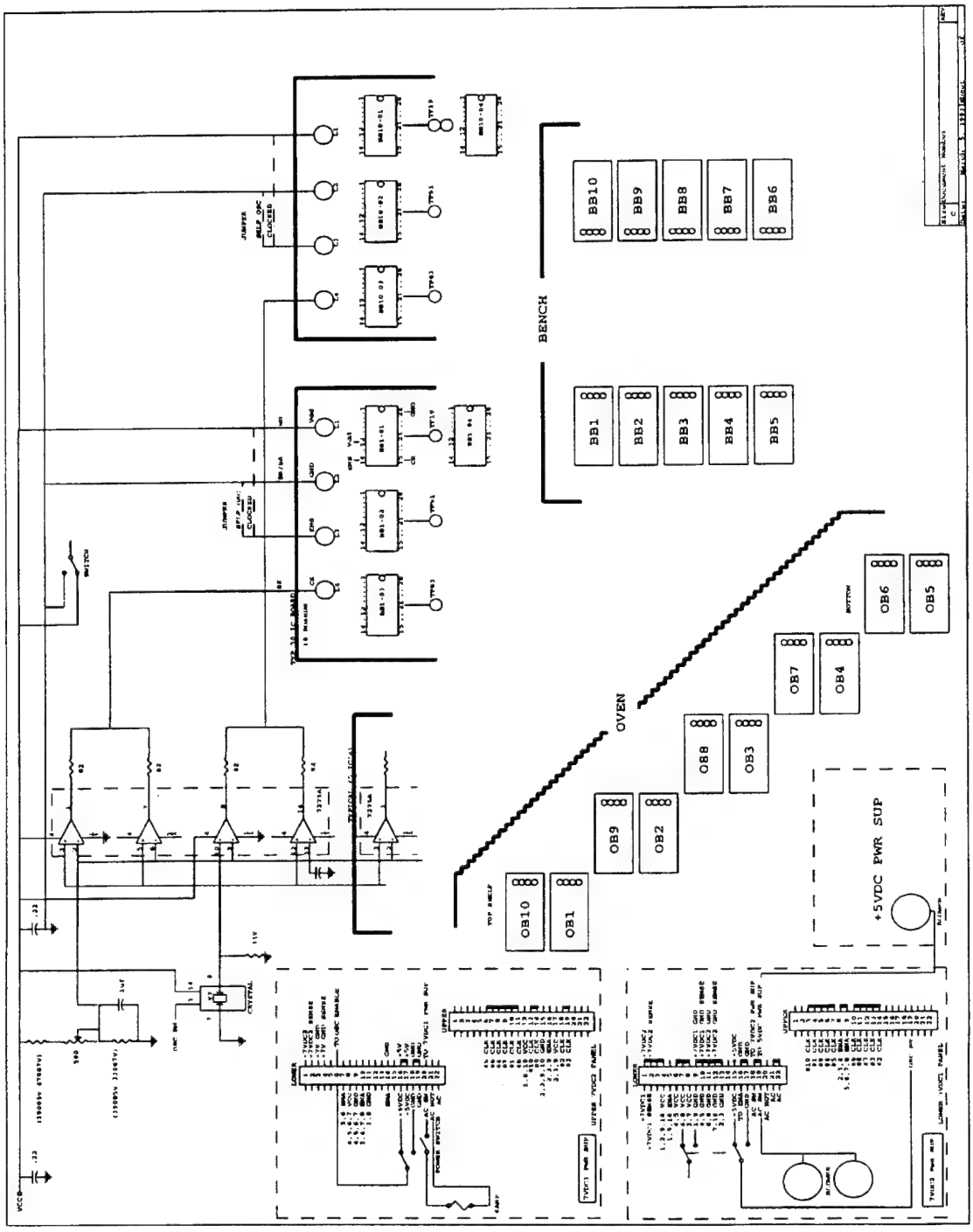

Figure 6: Test fixture power supply and clock driver hardware schematic diagram.

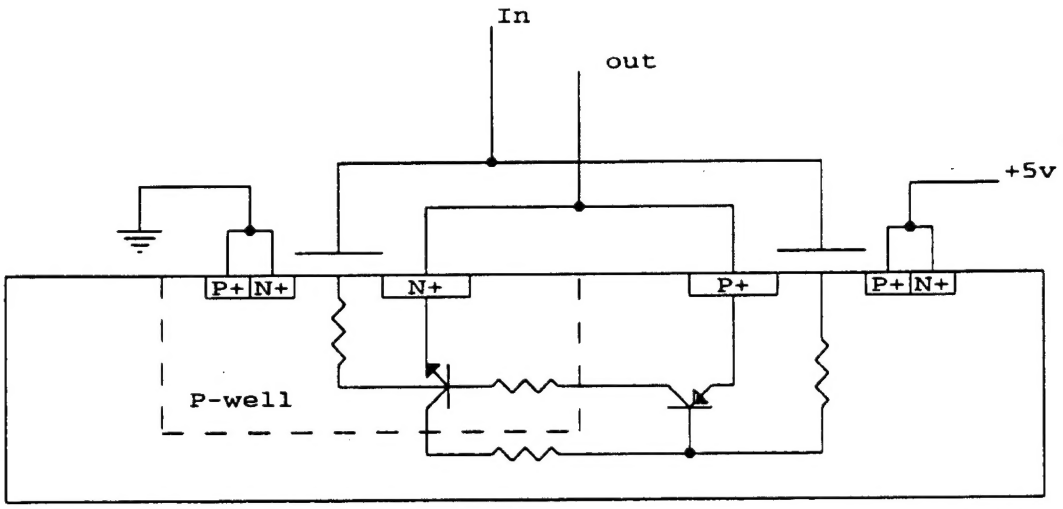

Figure 7: Latch-up Triggering by gate oxide failure. Parasitic BJT's are shown in a CMOS inverter Cross section diagram. The transistor diagram inside this figure illustrates the equivalent latch-up circuit. An oxide breakdown will provide a resistive path to the base of either the NPN or PNP transistor which will serve as the trigger for latch-up.

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